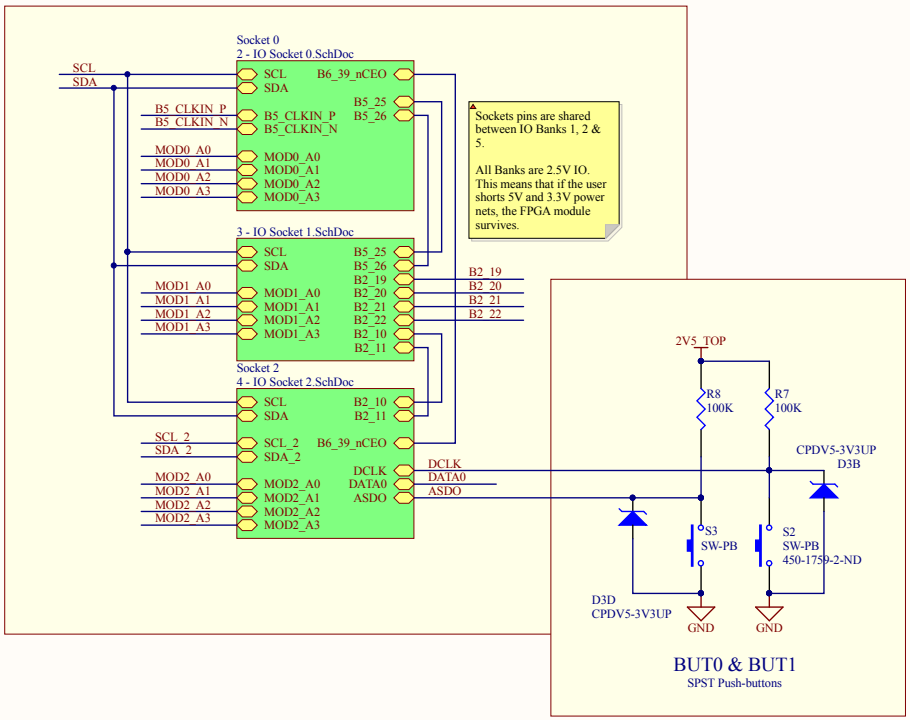
Revision History

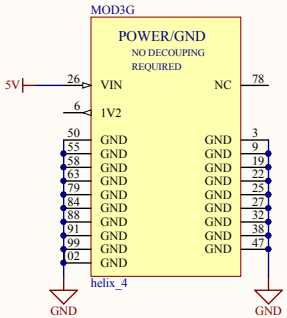
Project: helix_4 Rev C
PN: helix_4_ms_rev_e
Document Title: Multiple Sheild Dev Board for helix_4

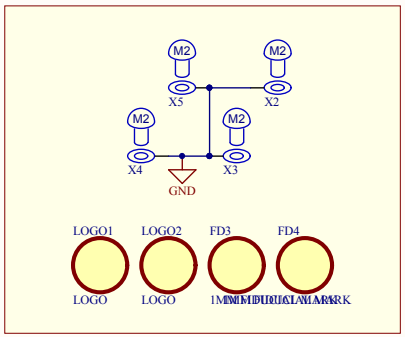
Description:
Access 3 Arduino Uno Sheilds with helix_4

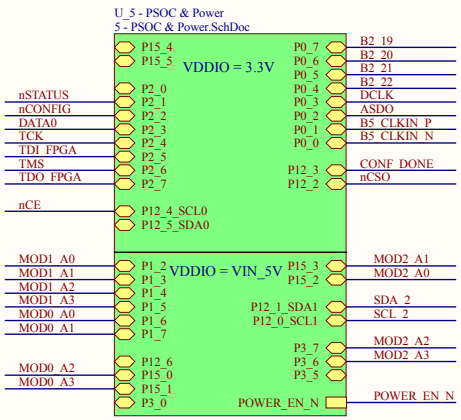
Revision History

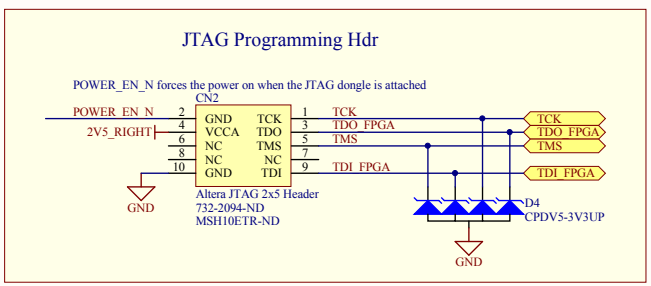
Rev A	B. Singer	16/02/2013	Released
Rev B	B. Singer	08/04/2013	Footprint changes
Rev C	B. Singer	25/04/2013	Repinning, removed gnd pad
Rev D	B. Singer	10/05/2013	VCC select per socket Removed all analog input pins Extra button, mod1 now all D's Move TXS's, I2C buffer per socket
Rev E	B. Singer	31/07/2013	Added PSOC, routed AN pins

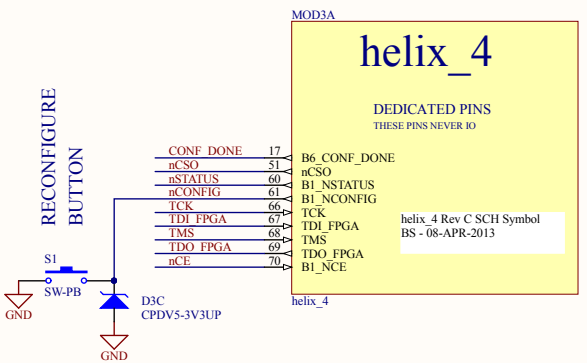


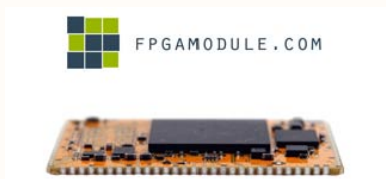








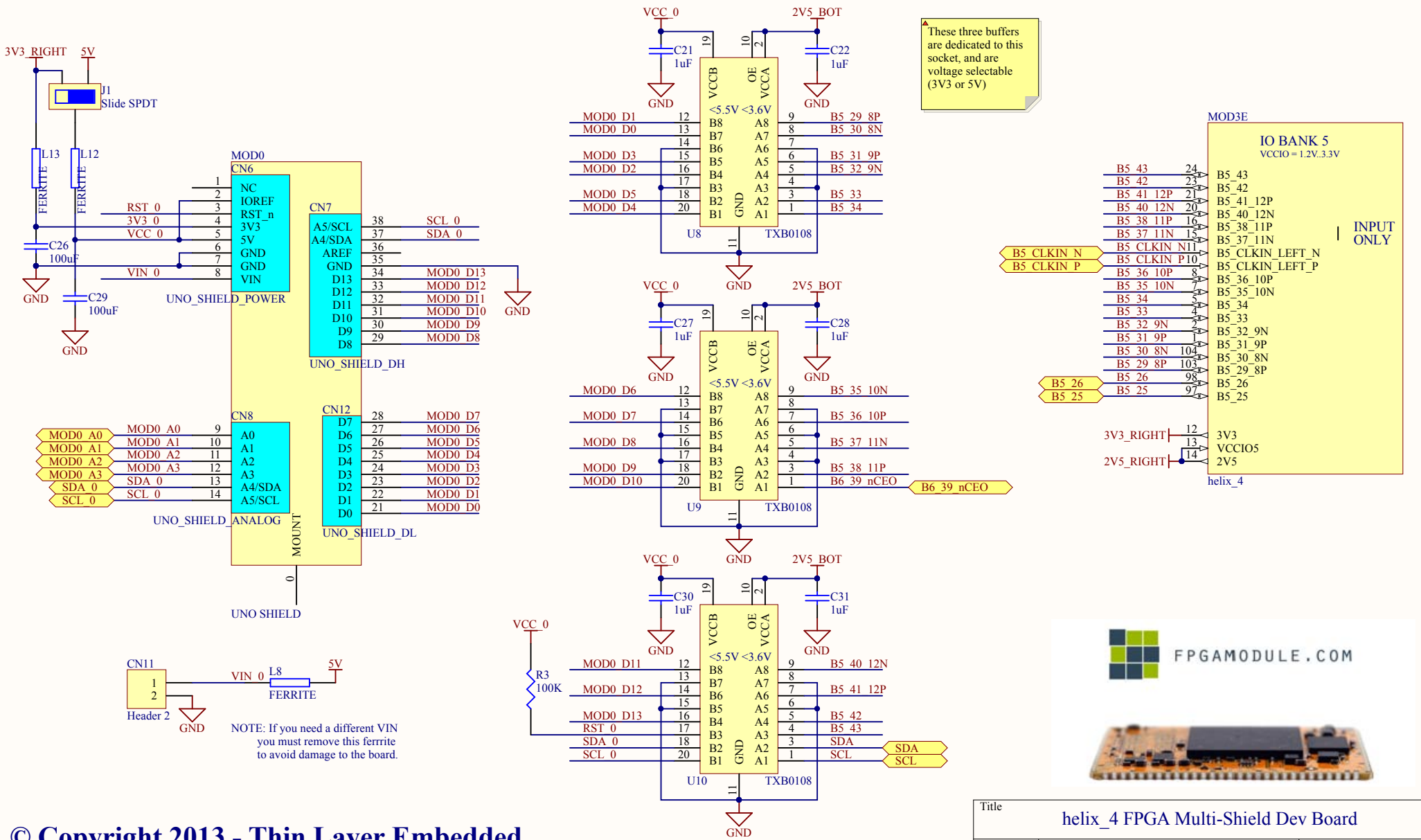




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Title	helix_4 FPGA Multi-Shield Dev Board	
Size: A3	Number: Page 1 - Top & Misc	Revision: Rev E
Date: 14/08/2013		Sheet of
File: D:\Google_Drive\..\1 - Top.SchDoc		Drawn By:



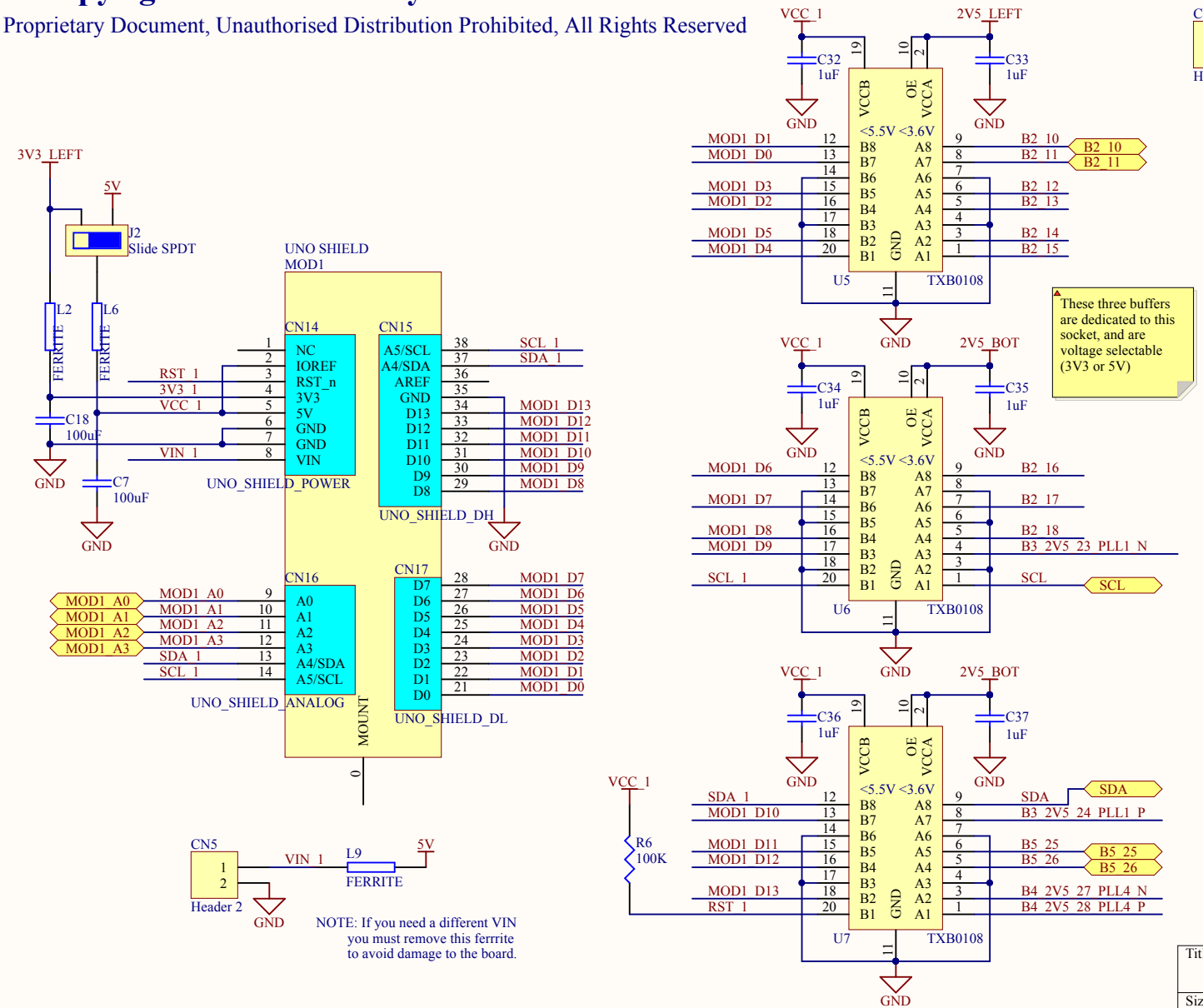
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Title	helix_4 FPGA Multi-Shield Dev Board	
Size: A4	Number: Page 2 - Socket 0	Revision: Rev E
Date: 14/08/2013	Sheet of	
File: D:\Google Drive\..\2 - IO Socket 0.SchDoc	Drawn By:	

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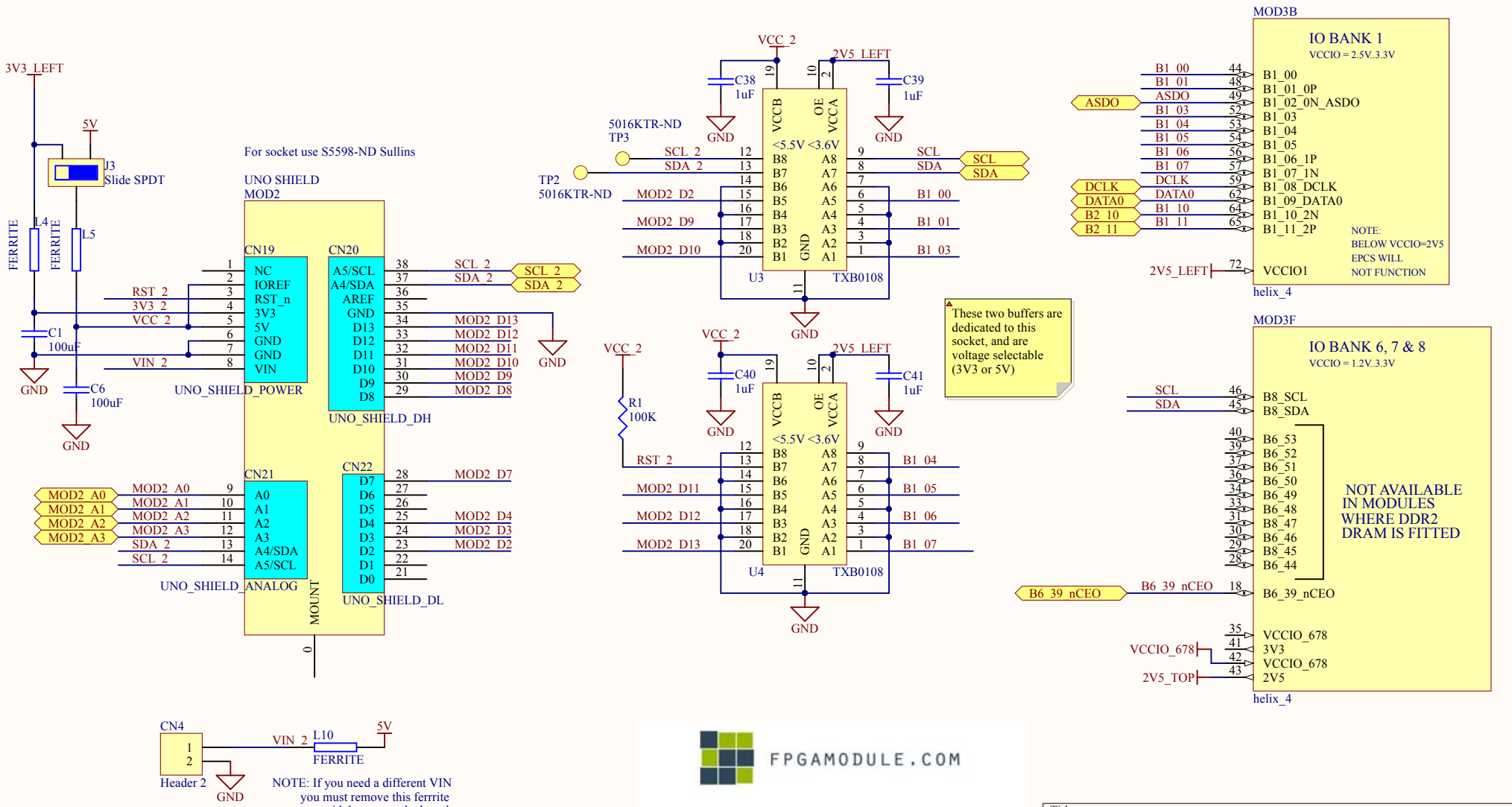
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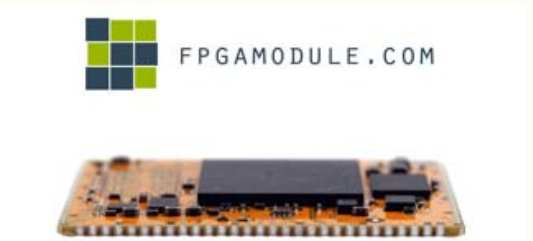


Title	helix_4 FPGA Multi-Shield Dev Board	
Size: A4	Number: Page 3- Socket 1	Revision: Rev E
Date: 14/08/2013	Sheet of	
File: D:\Google Drive\..\3 - IO Socket 1.SchDoc	Drawn By:	

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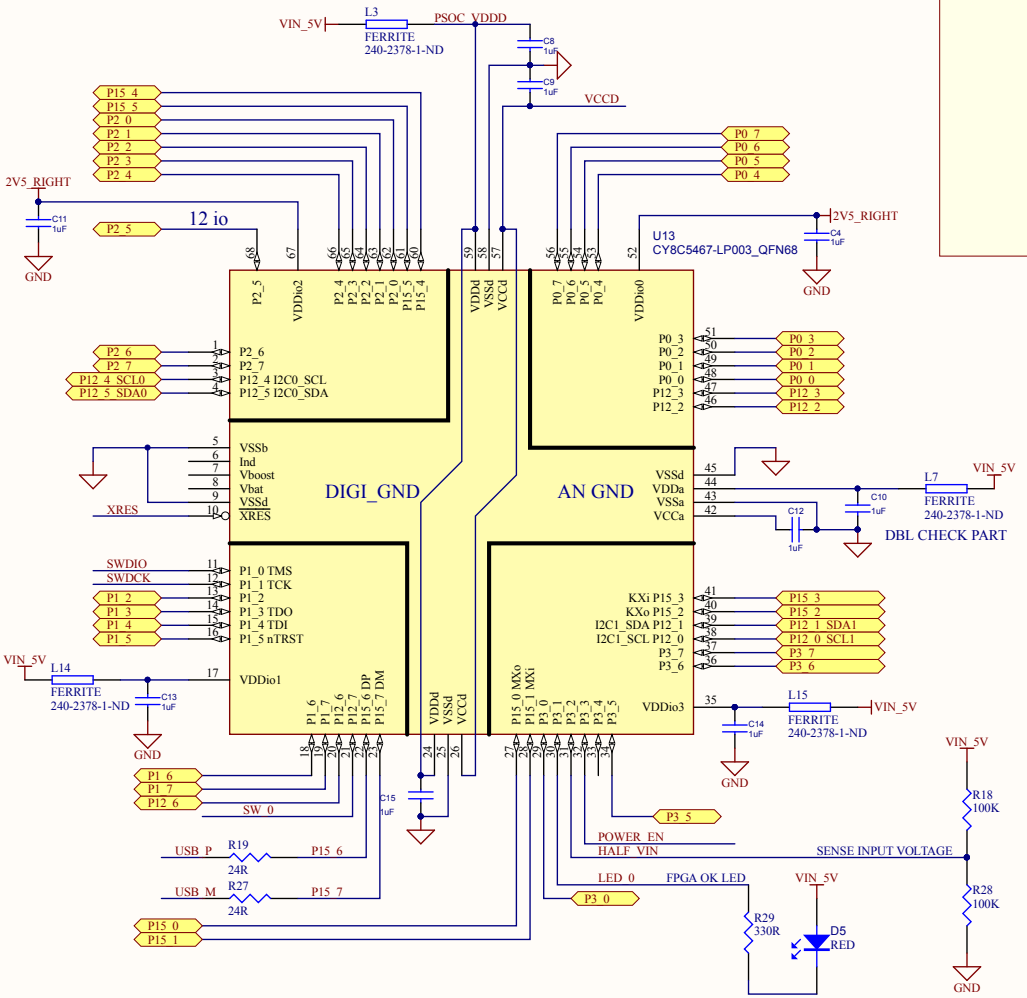
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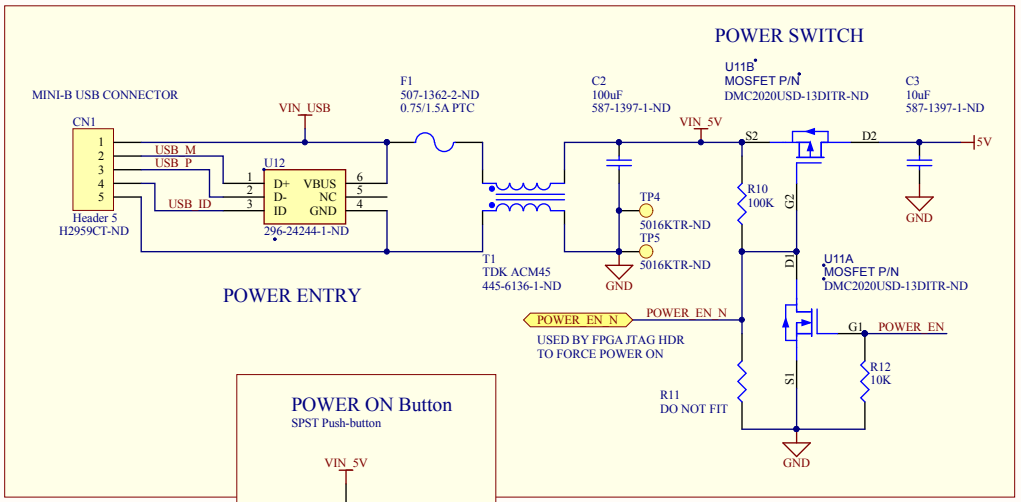


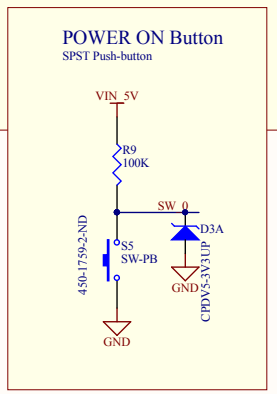


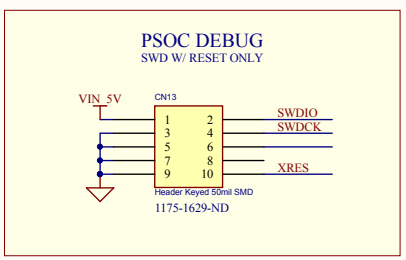
Title	helix_4 FPGA Multi-Shield Dev Board	
Size: A4	Number: Page 4 - Socket 2	Revision: Rev E
Date: 14/08/2013	Sheet of	
File: D:\Google Drive\..\4 - IO Socket 2.SchDoc	Drawn By:	

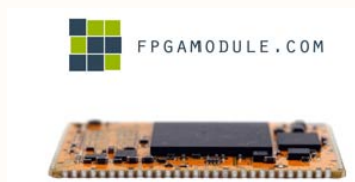
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FPGA



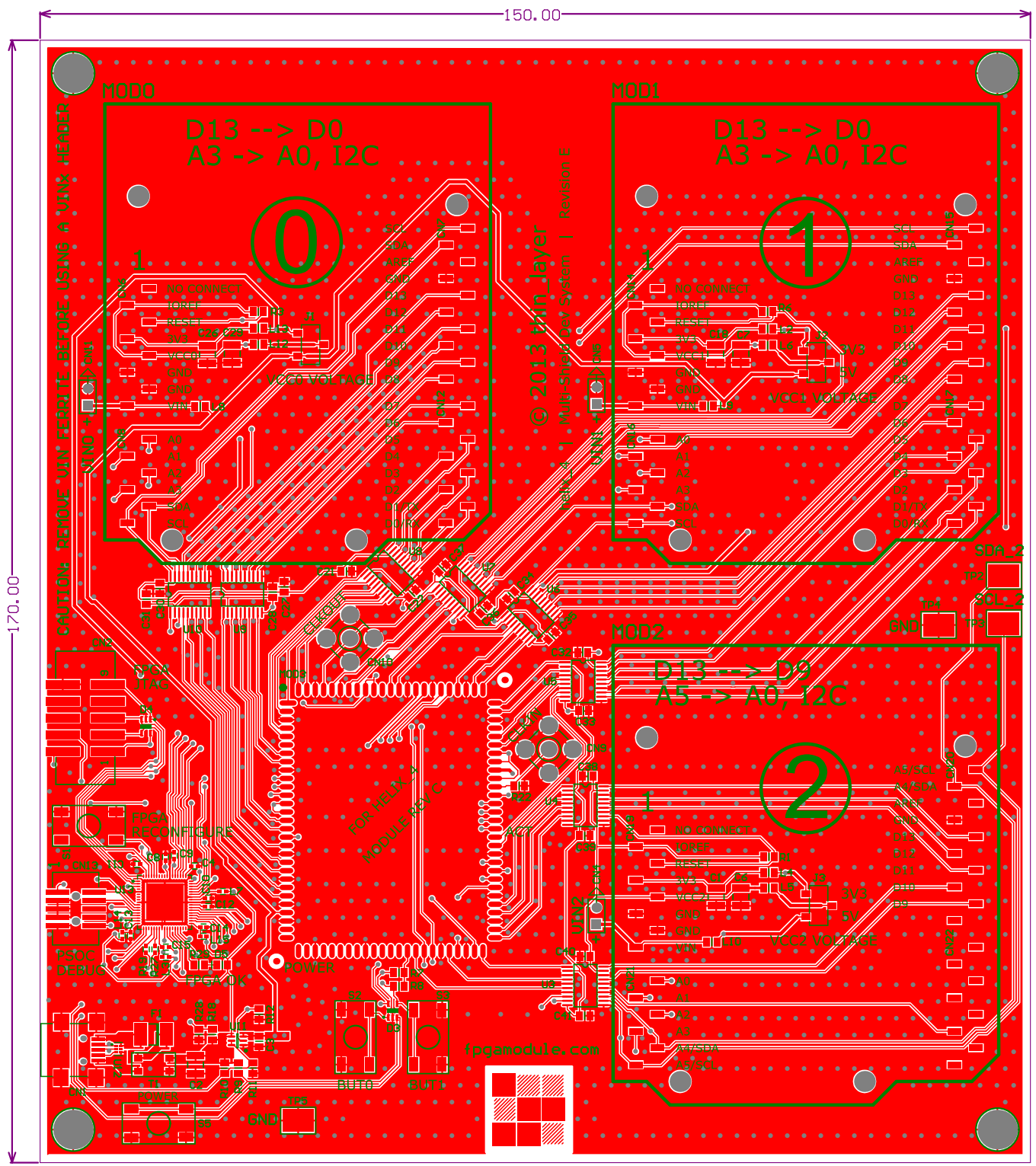








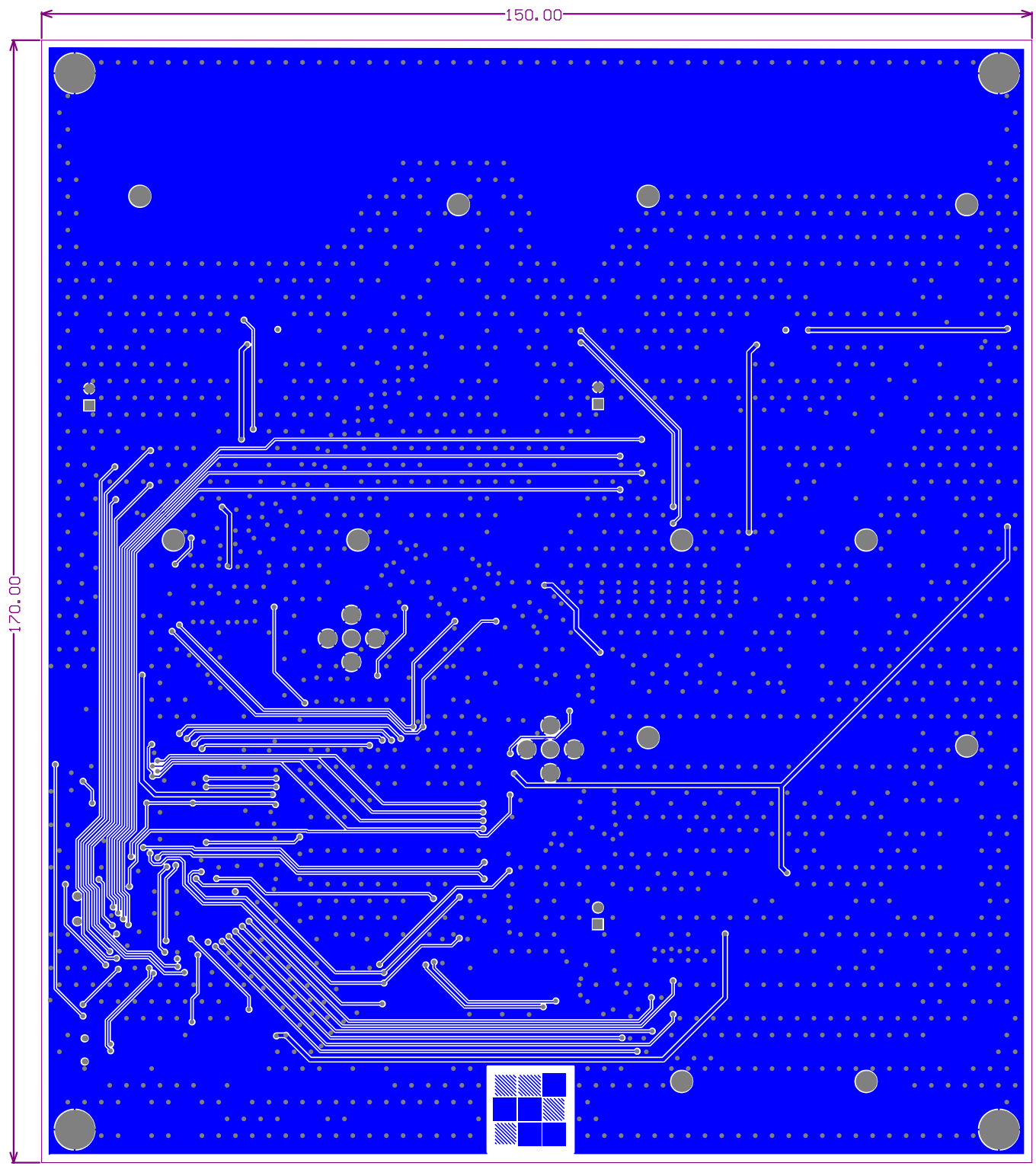
Title: helix_4 FPGA Multi-Shield Dev Board		
Size: A3	Number: Page 5 - PSOC & Power	Revision: Rev E
Date: 14/08/2013	Sheet of	
File: D:\Google_Drive\...\5 - PSOC & Power.SchDoc	Drawn By:	



TOP SILK

TOP COPPER LAYER

BOARD OUTLINE



BOTTOM COPPER LAYER

BOARD OUTLINE