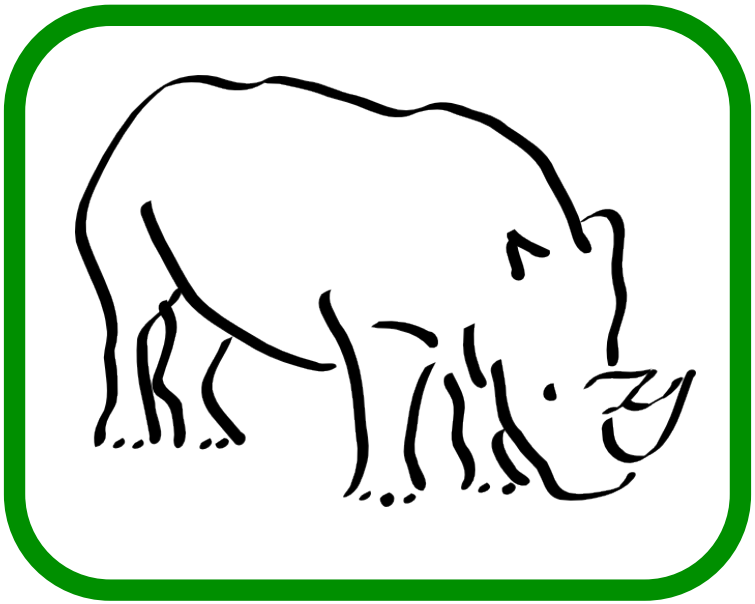


UCT Software-Defined
Radio Research Group



RHINO

Reconfigurable Hardware Interface for computatioN and radiO

TEXAS INSTRUMENTS

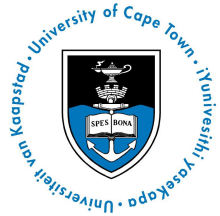
XILINX®

SKA SOUTH AFRICA
SQUARE KILOMETRE ARRAY

UCT SDRRG Team

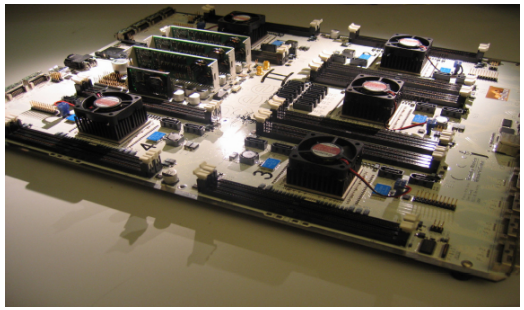


- UCT Faculty:
  - Alan Langman
  - Mike Inggs
  - Simon Winberg
- PhD Students:
  - Brandon Hamilton
- MSc Students:
  - Bruce Raw
  - Gordon Inggs
  - Simon Scott
  - Joseph Wamicha

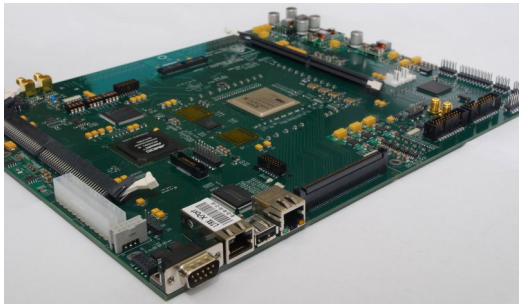


UCT Software-Defined
Radio Research Group

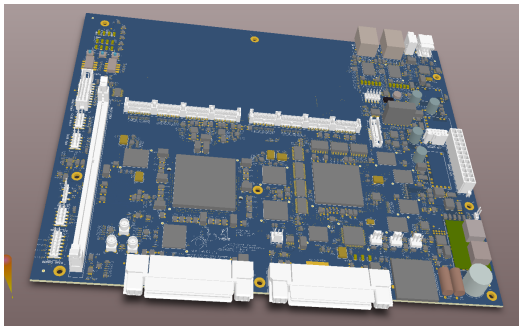
Current CASPER Hardware



BEE2 $$$$



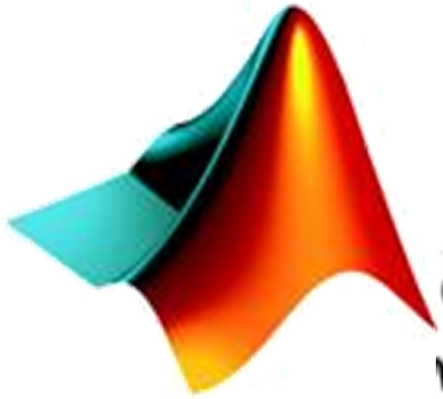
ROACH $$$



ROACH 2 $$$$$$

*Disclaimer: Alan made me include this slide

Current Software



MATLAB®
SIMULINK®

=

$ $ $ $ $ $

Need for low-cost solution



- Great boards and (relatively) easy-to-use toolchain
- But expensive, so not accessible to smaller research groups
- Lack of HPC skills in South Africa
- Low-cost h/w and s/w solution needed
- Enlarge CASPER community

Requirements



- Low cost hardware
  - Simple design rather than low performance
- Open-source software
- Easy to learn and use
- Compatible with existing h/w and s/w
- Target software-defined radio apps

Proposed Solution



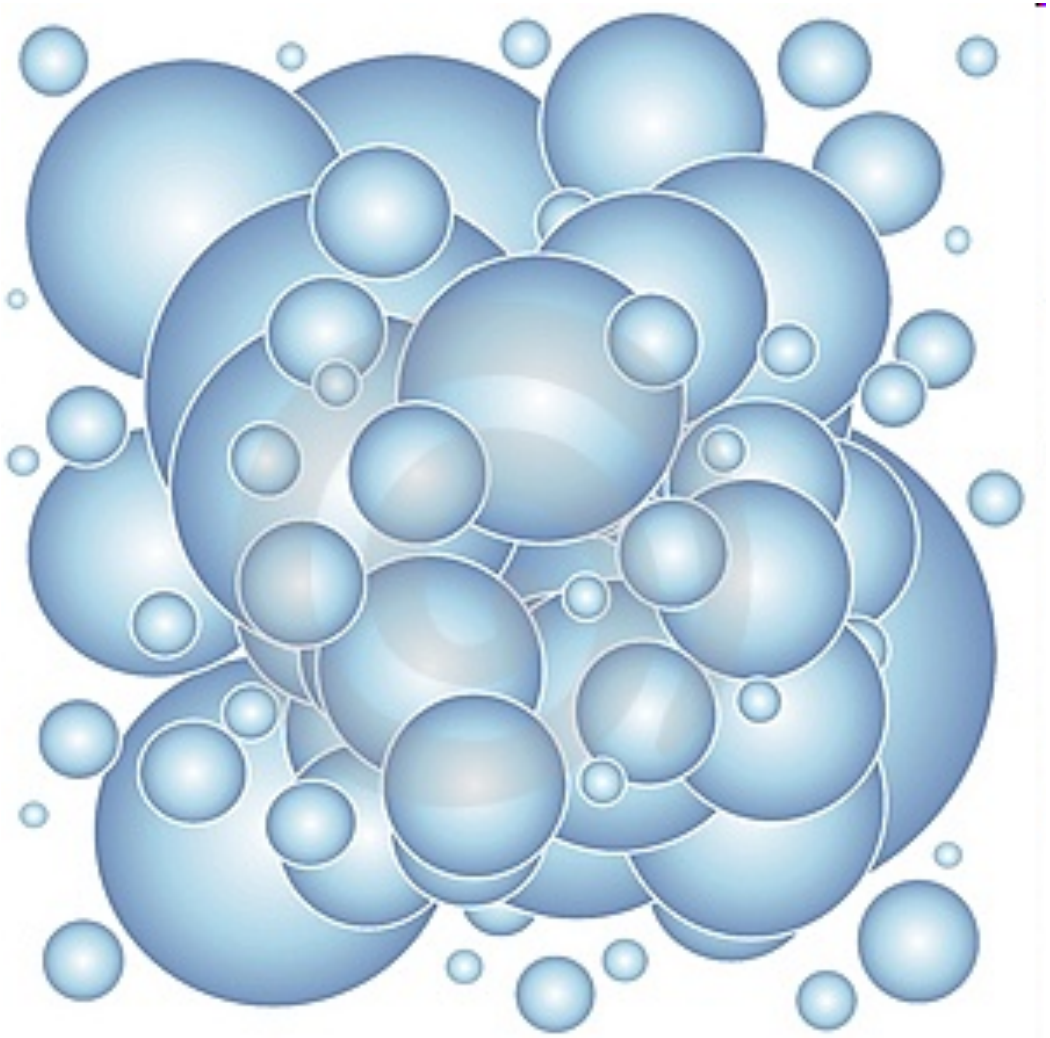
- Similar to existing CASPER hardware (FPGA + processor)
- Xilinx Spartan-6 FPGA
  - Sufficient performance for most apps, but lower cost
- TI ARM Cortex-A8 processor
  - Large support community
- FPGA Mezzanine Card (FMC) connector
- Python-based toolchain

Throw them all in a pot…

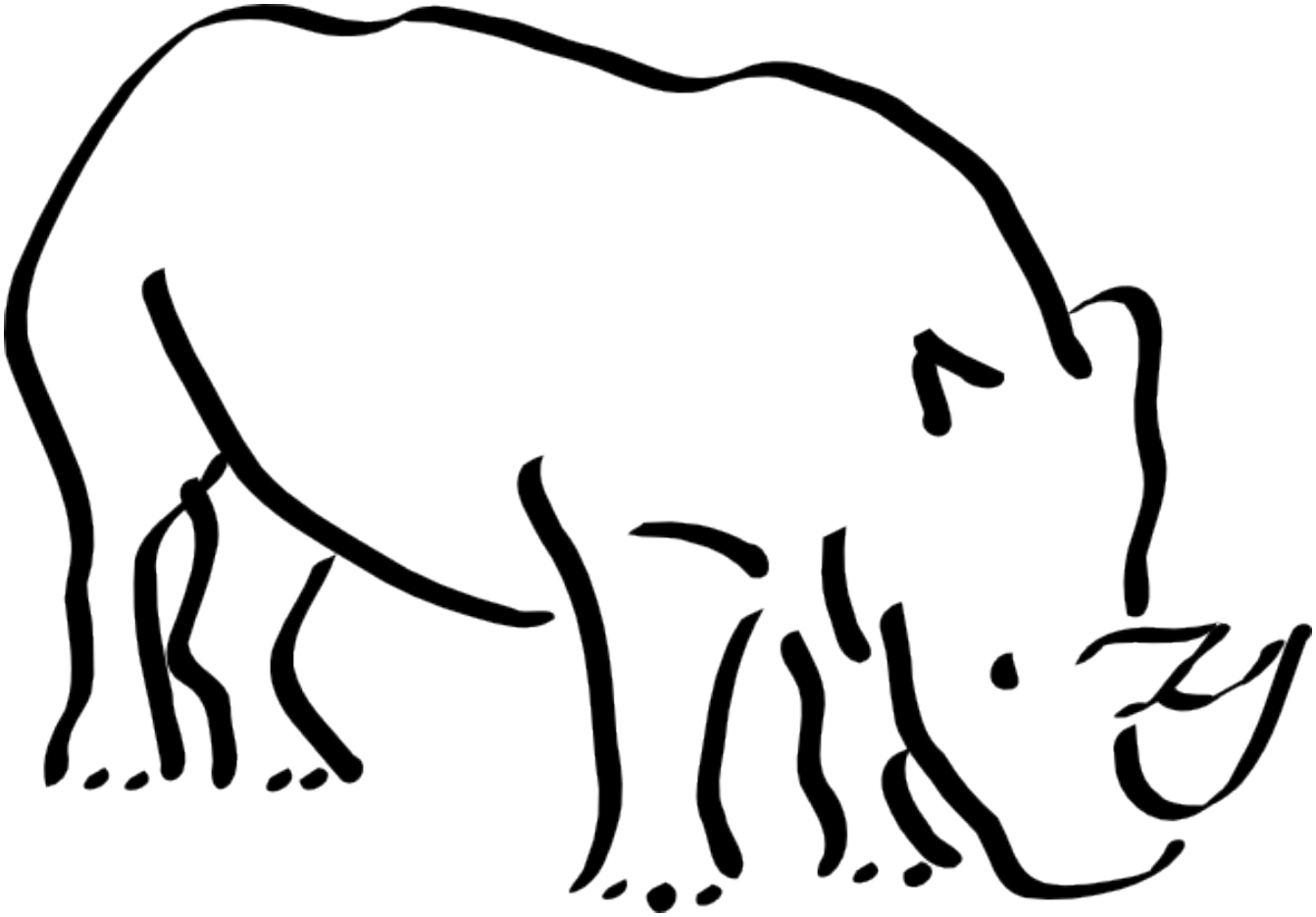
RHINO
Reconfigurable Hardware Interface for computatioN and radiO



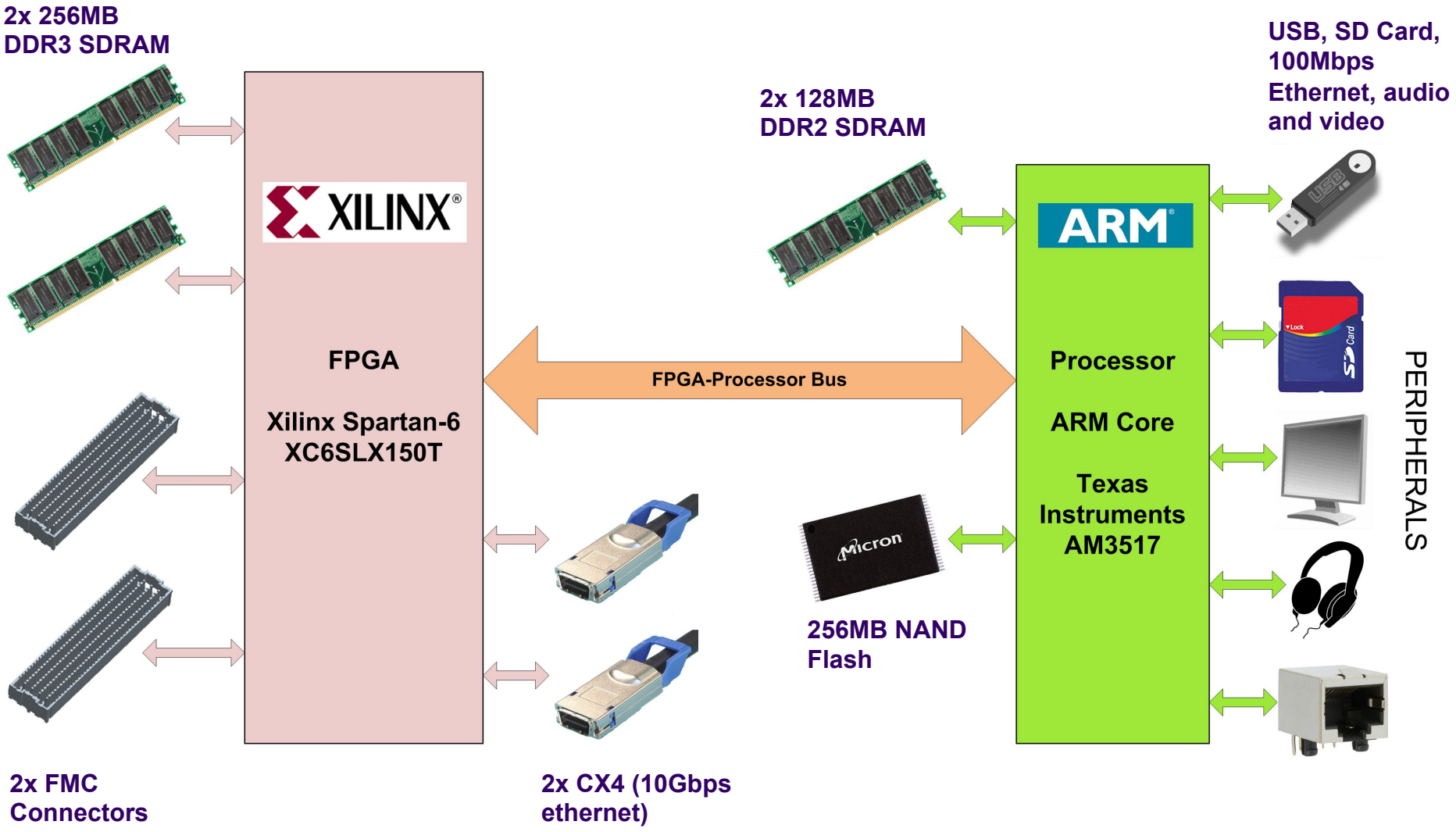
Mix them up…



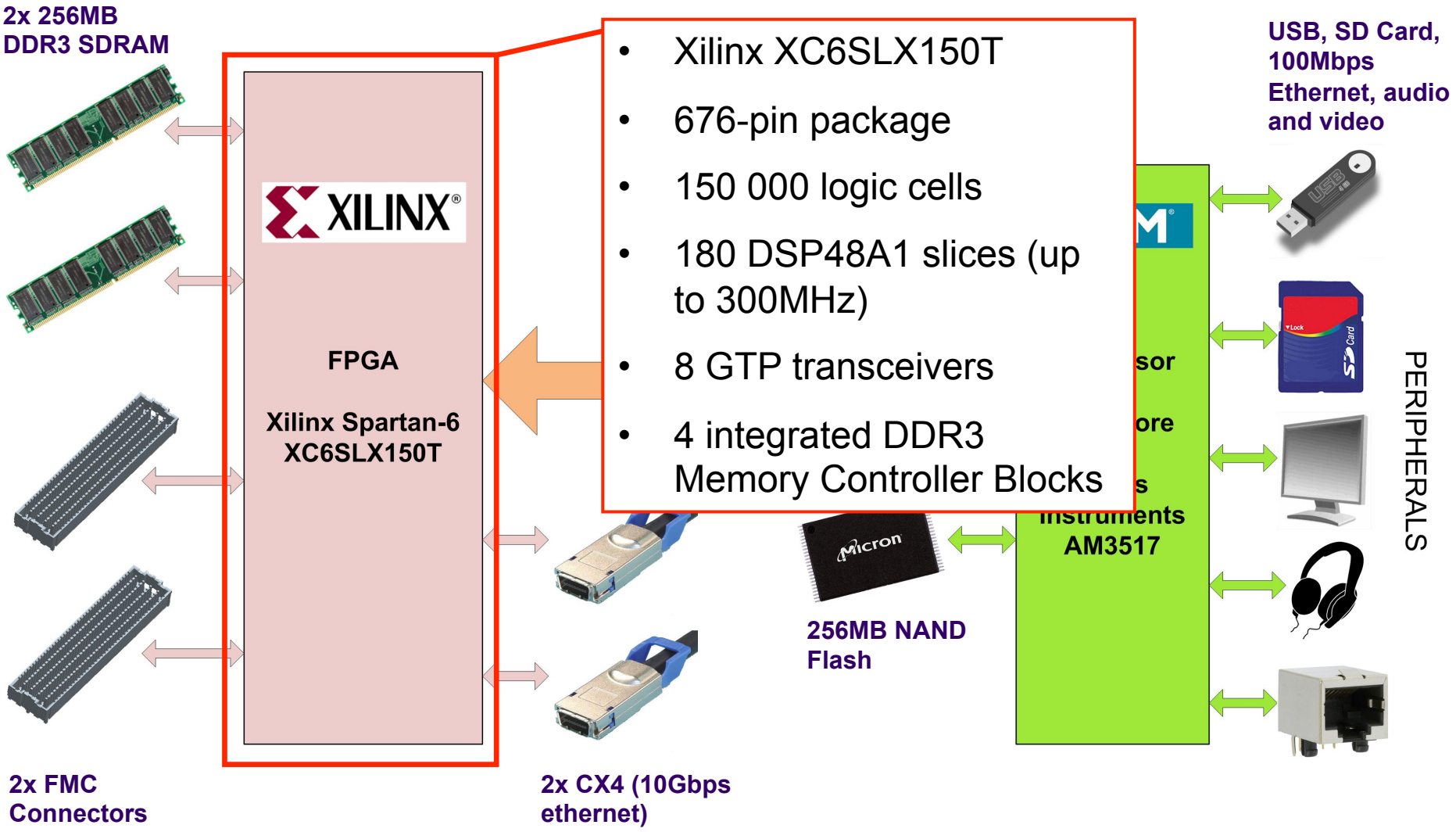
And you get a Rhino!



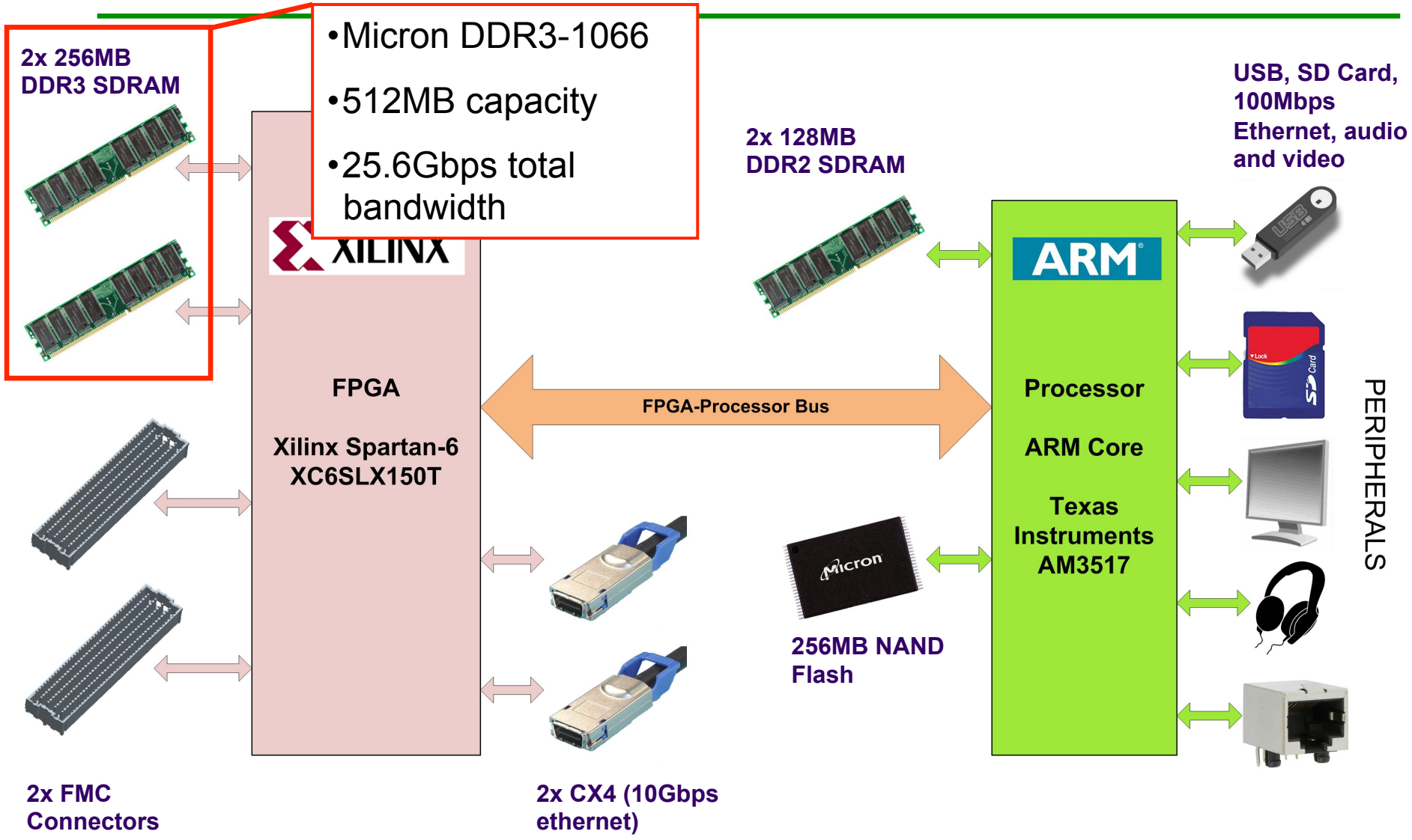
Rhino Architecture



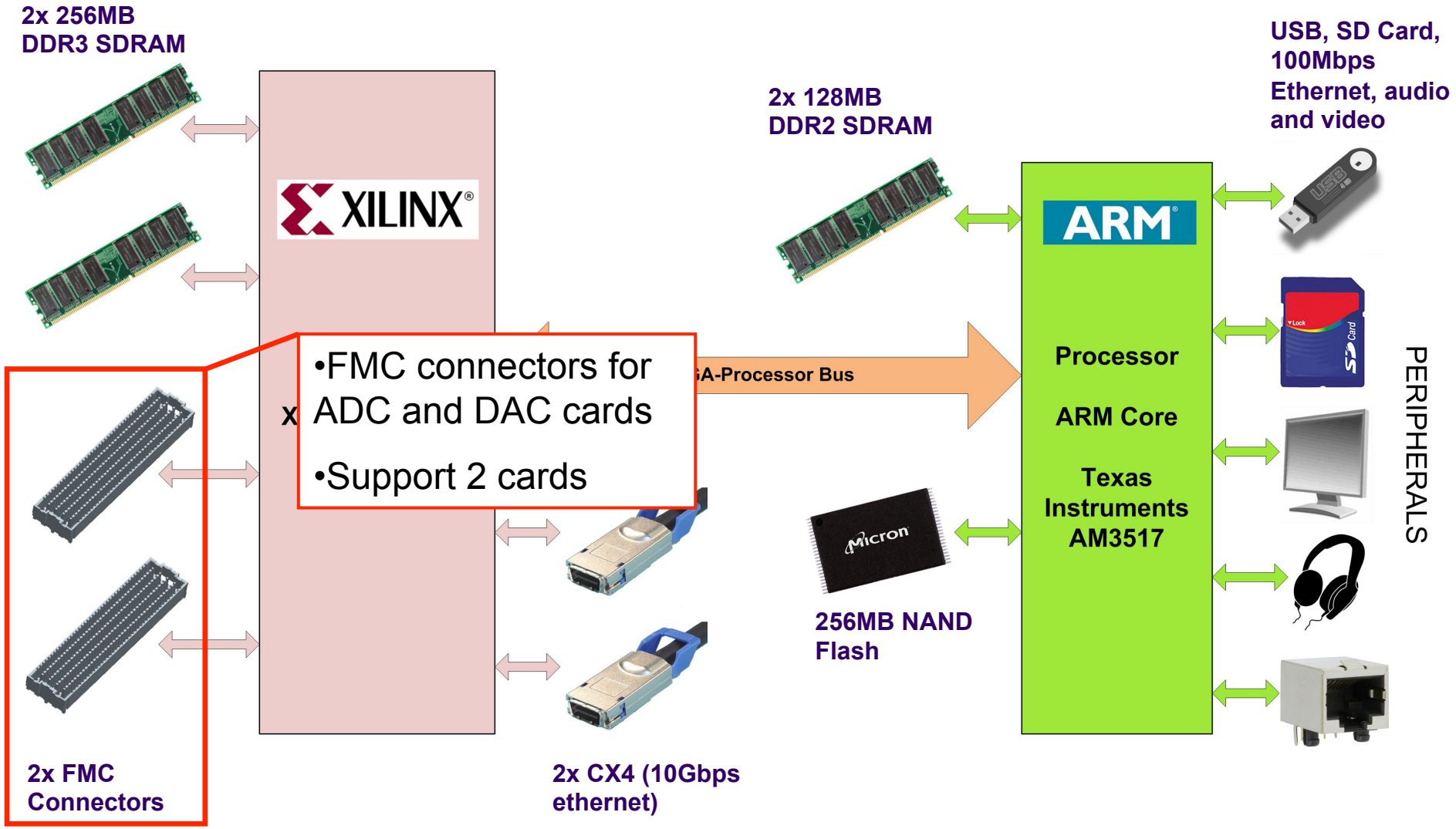
Xilinx Spartan-6



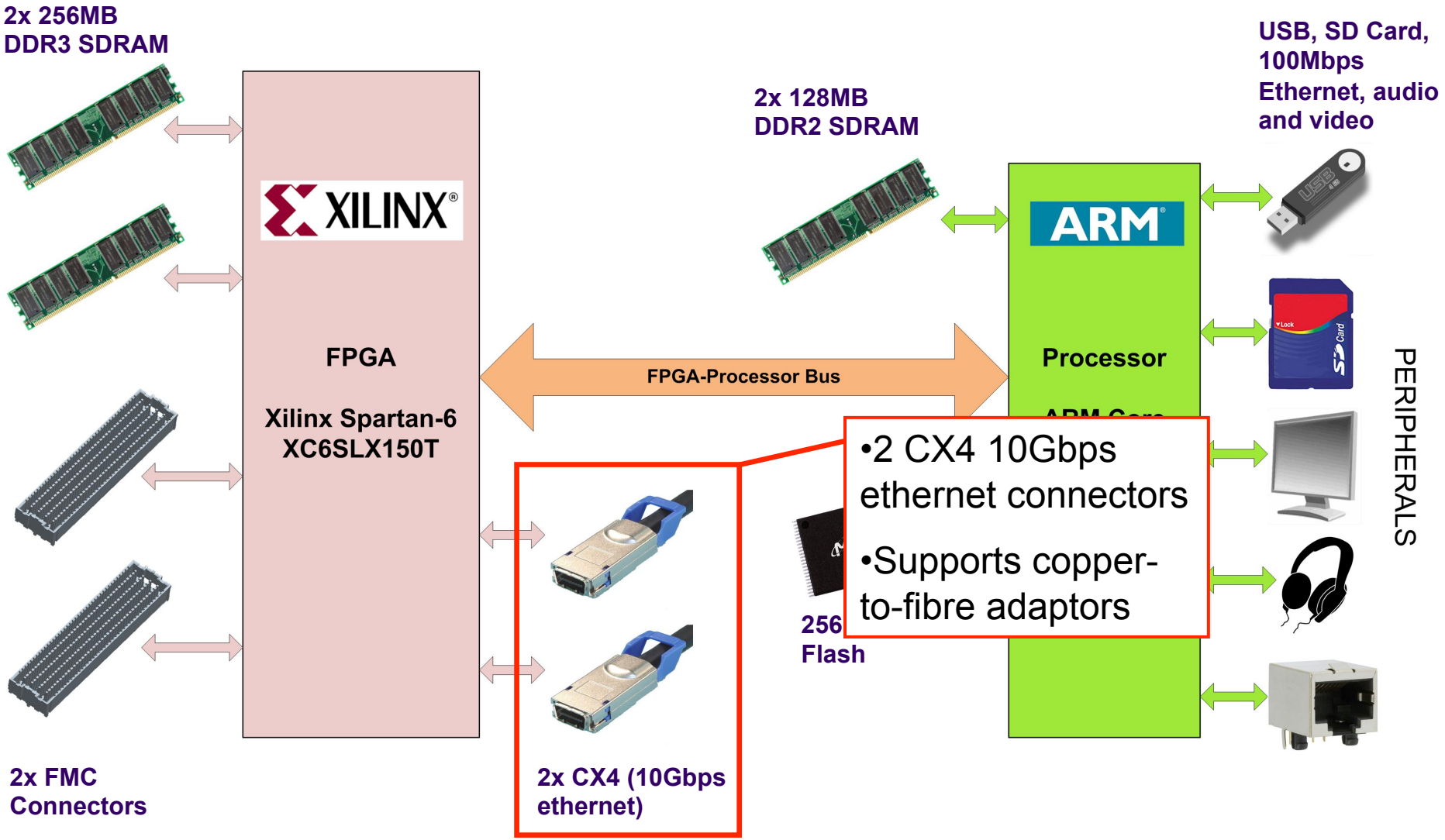
DDR2 SDRAM


2x 256MB
DDR3 SDRAM
•Micron DDR3-1066
•512MB capacity
•25.6Gbps total bandwidth
XILINX
FPGA
Xilinx Spartan-6
XC6SLX150T
2x FMC
Connectors
2x CX4 (10Gbps
ethernet)
FPGA-Processor Bus
2x 128MB
DDR2 SDRAM
ARM
Processor
ARM Core
Texas
Instruments
AM3517
Micron
256MB NAND
Flash
USB, SD Card,
100Mbps
Ethernet, audio
and video
PERIPHERALS

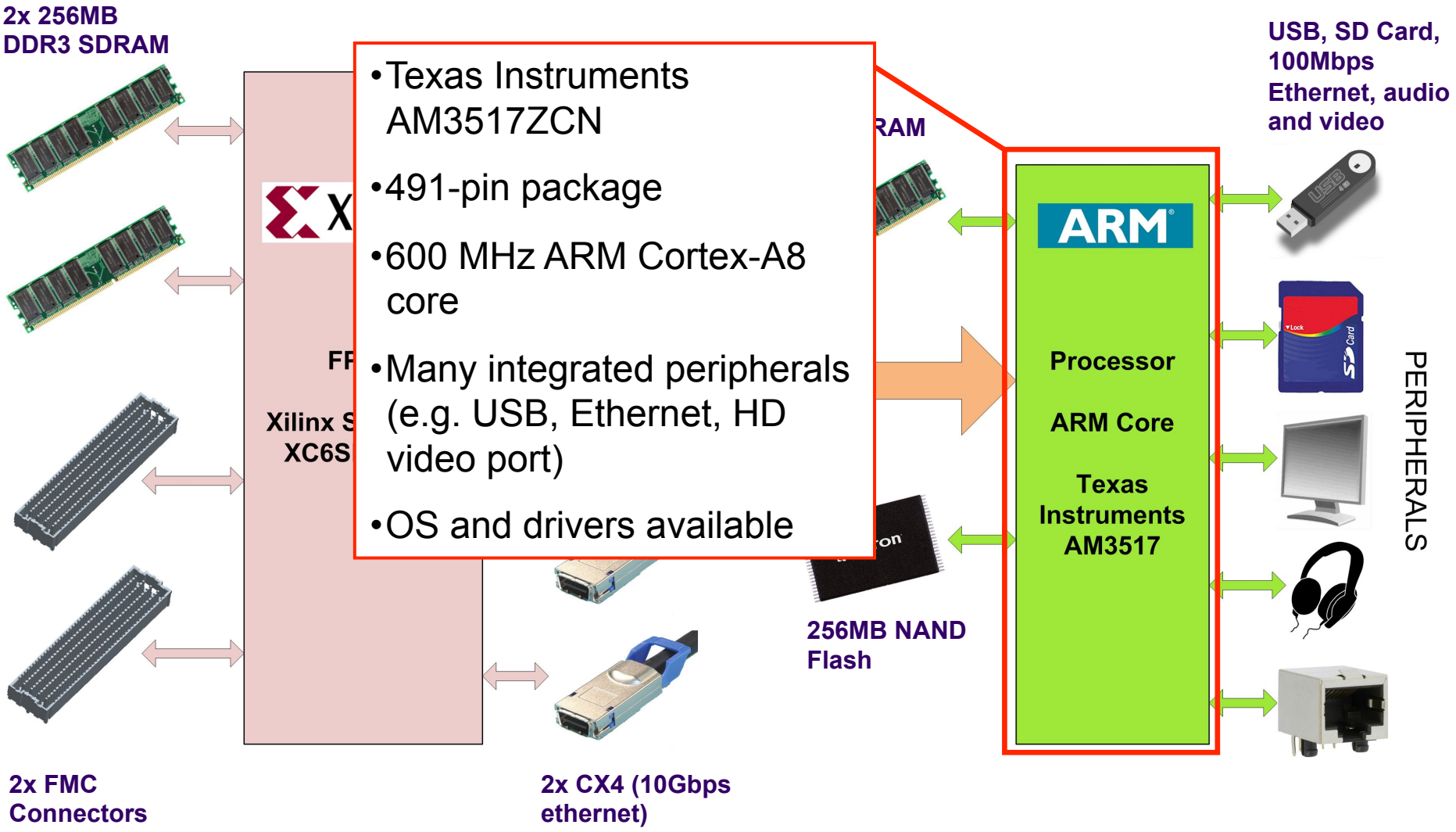
FMC ADC/DAC Connectors



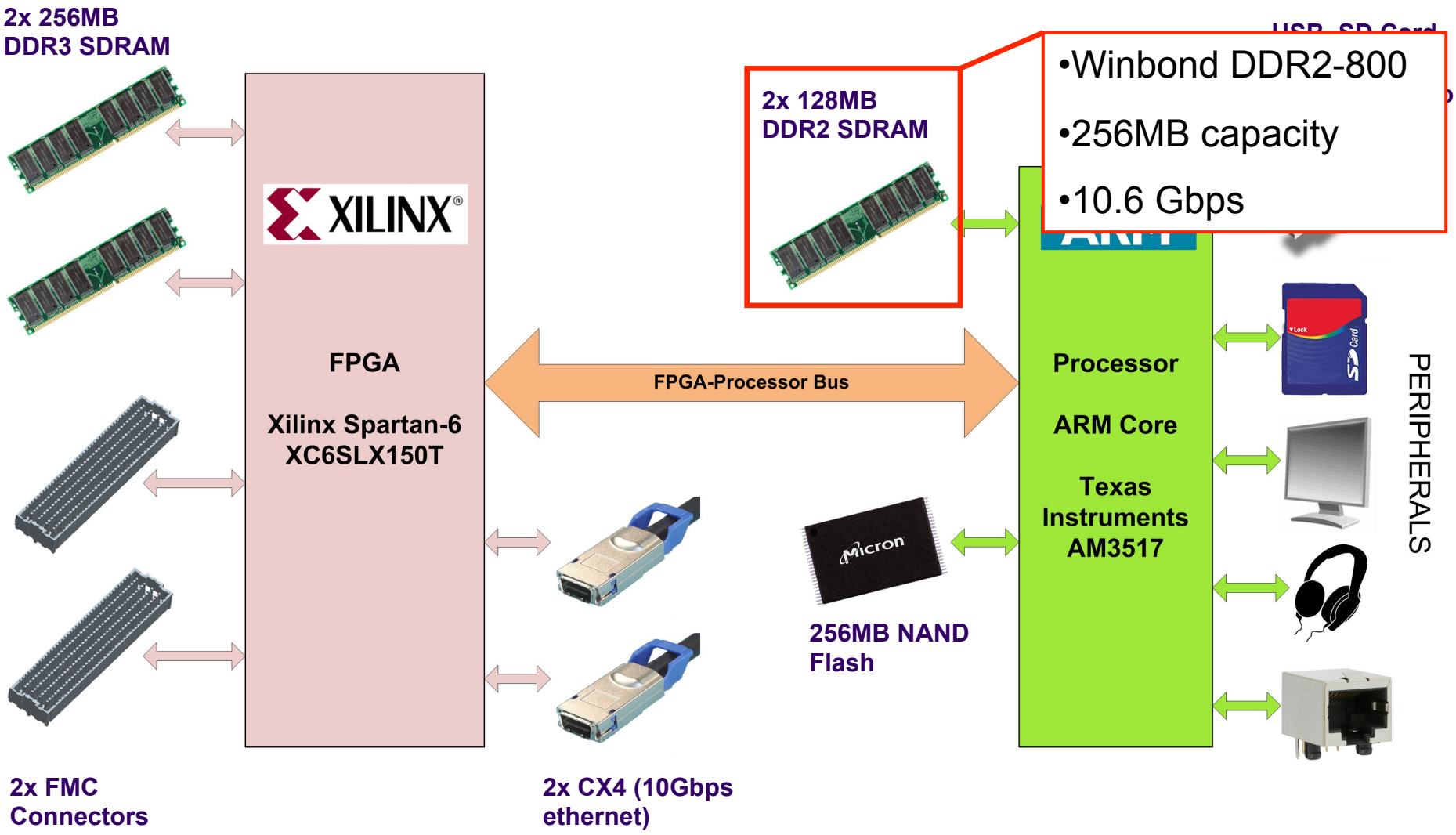
CX4 10Gbps Ethernet



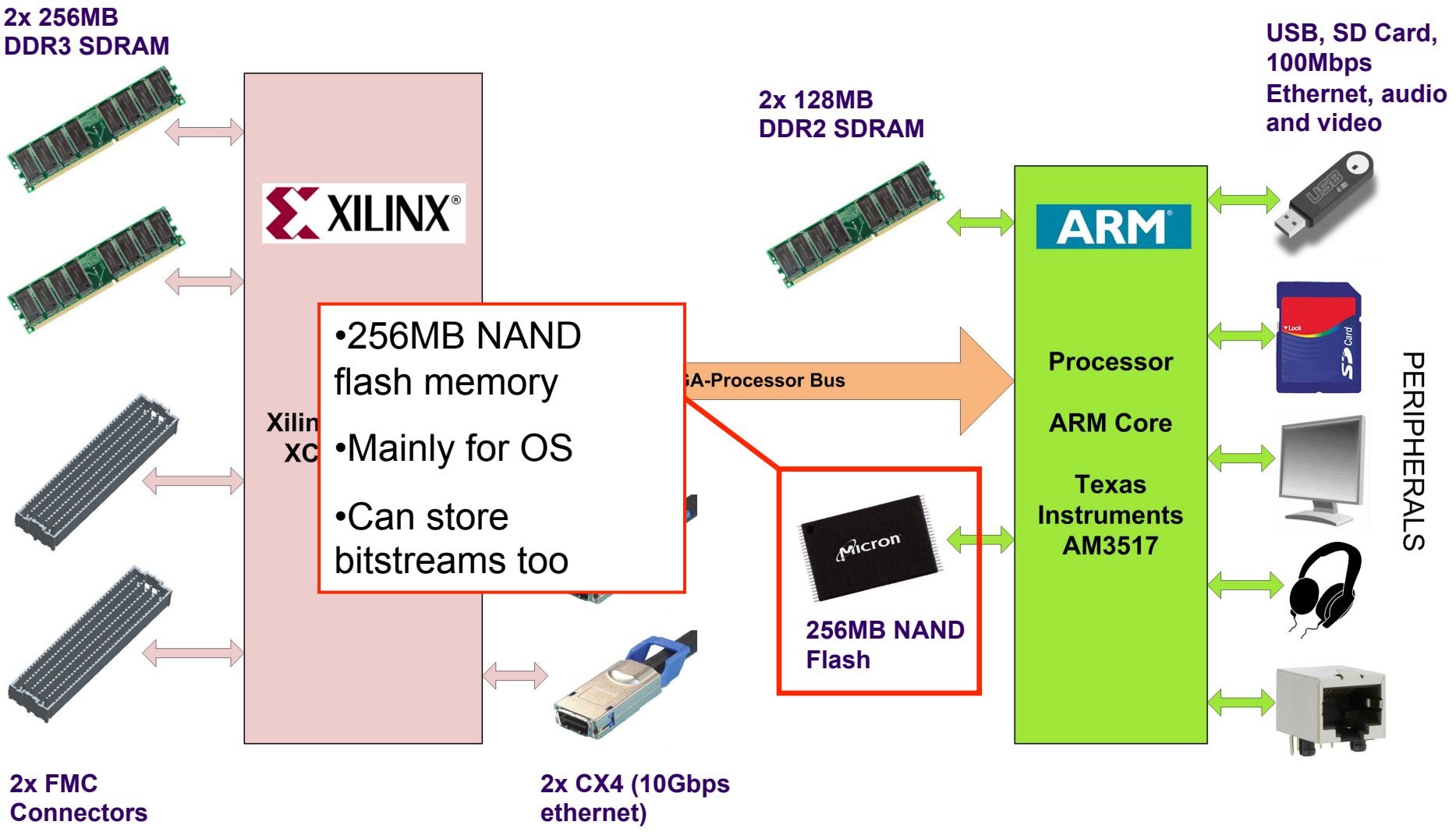
TI AM3517 ARM Cortex-A8



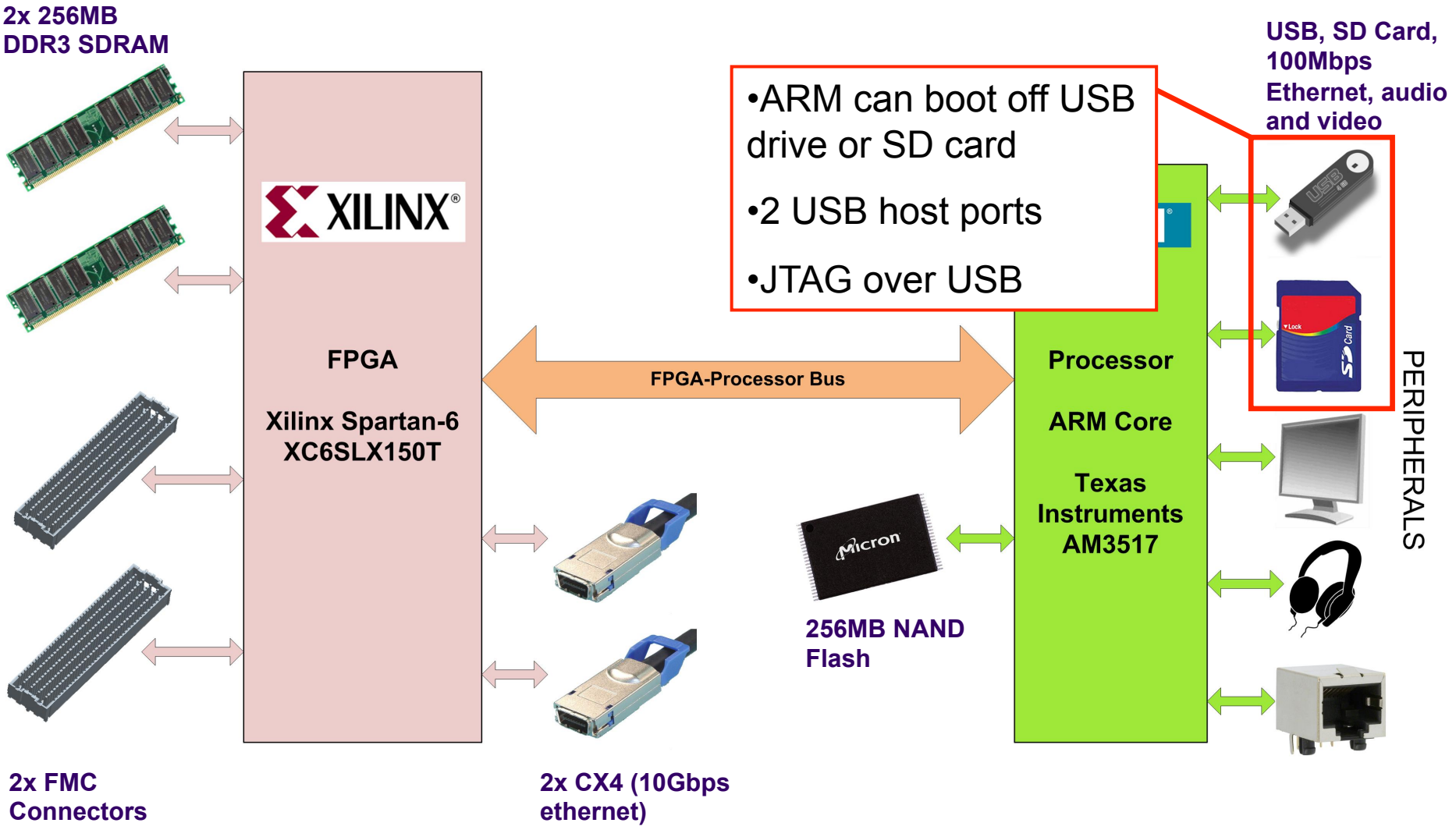
DDR2 SDRAM


2x 256MB
DDR3 SDRAM
XILINX
FPGA
Xilinx Spartan-6
XC6SLX150T
2x 128MB
DDR2 SDRAM
•Winbond DDR2-800
•256MB capacity
•10.6 Gbps
FPGA-Processor Bus
Processor
ARM Core
Texas
Instruments
AM3517
Micron
256MB NAND
Flash
PERIPHERALS
2x FMC
Connectors
2x CX4 (10Gbps
ethernet)

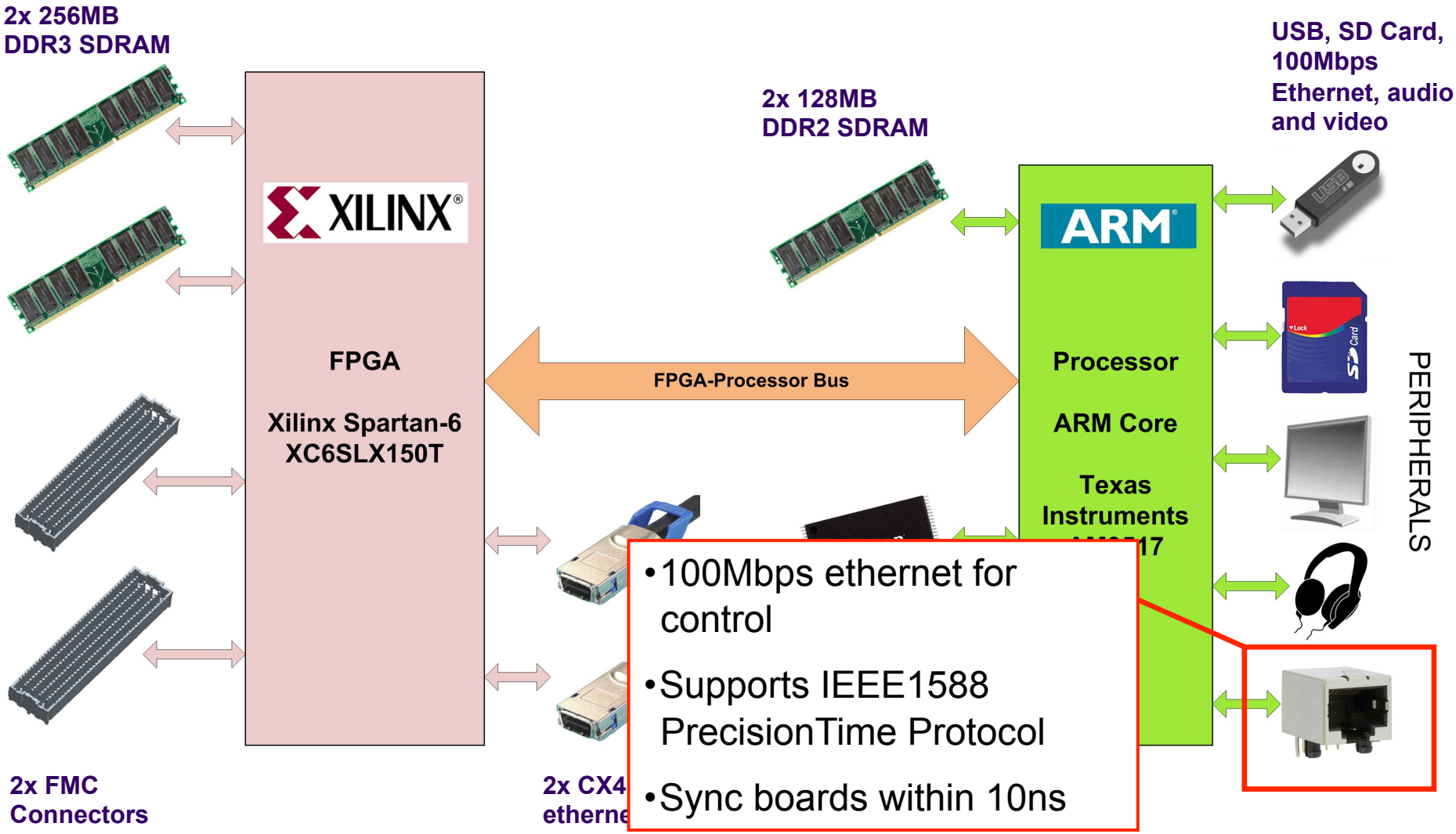
NAND Flash Memory



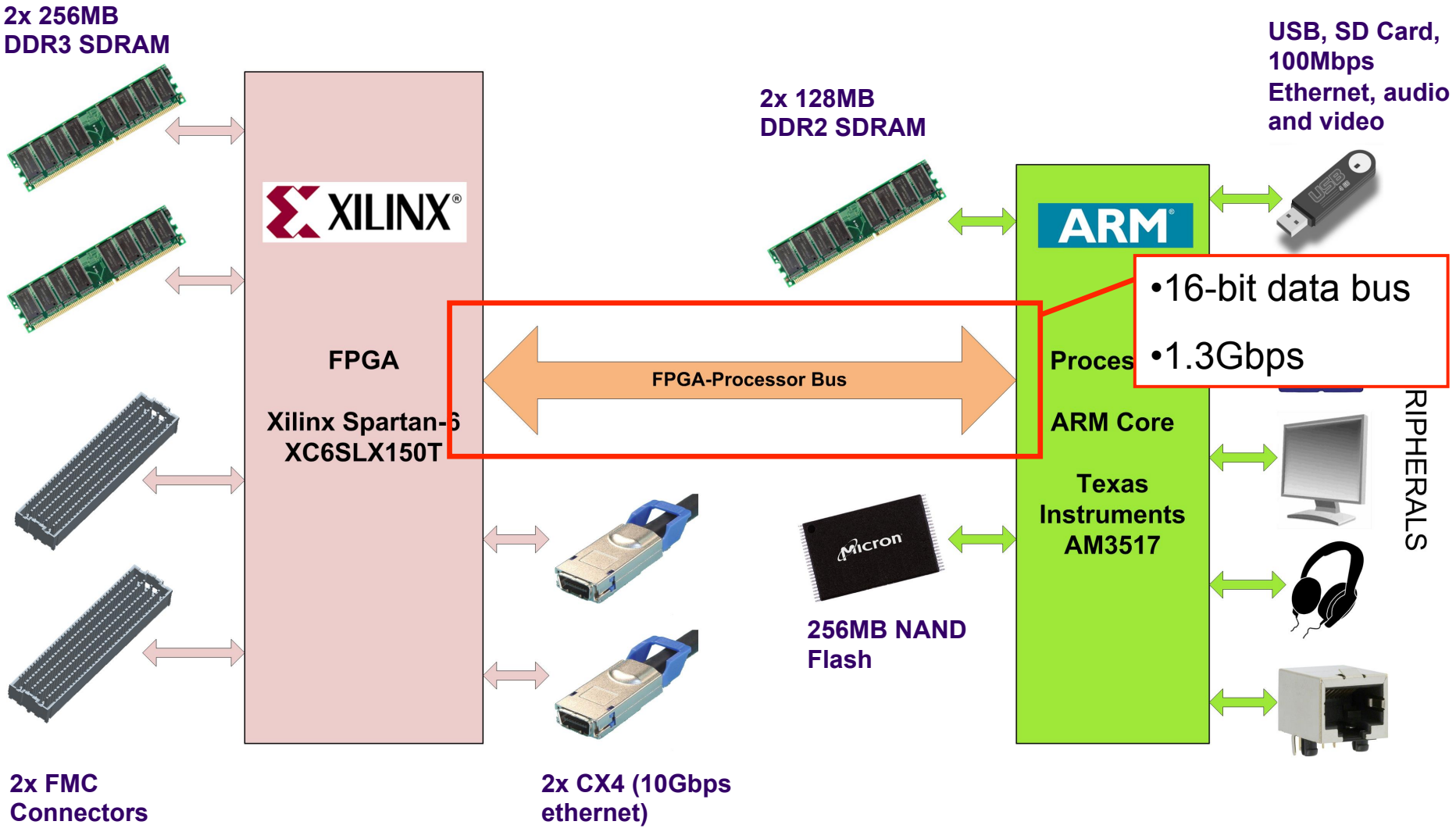
USB and SD Card



100Mbps Ethernet



FPGA-Processor Bus



FPGA Mezzanine Card (FMC)



- ANSI/VITA 57.1 standard
- Low-pin count:
  - 160 pin
  - 34 differential data pairs, 2 high-speed serial pairs
  - 2 (+4) clocks, I2C, JTAG
- High-pin count:
  - 400 pin
  - 80 differential data pairs, 20 high-speed serial pairs
  - 4 (+9) clocks, I2C, JTAG

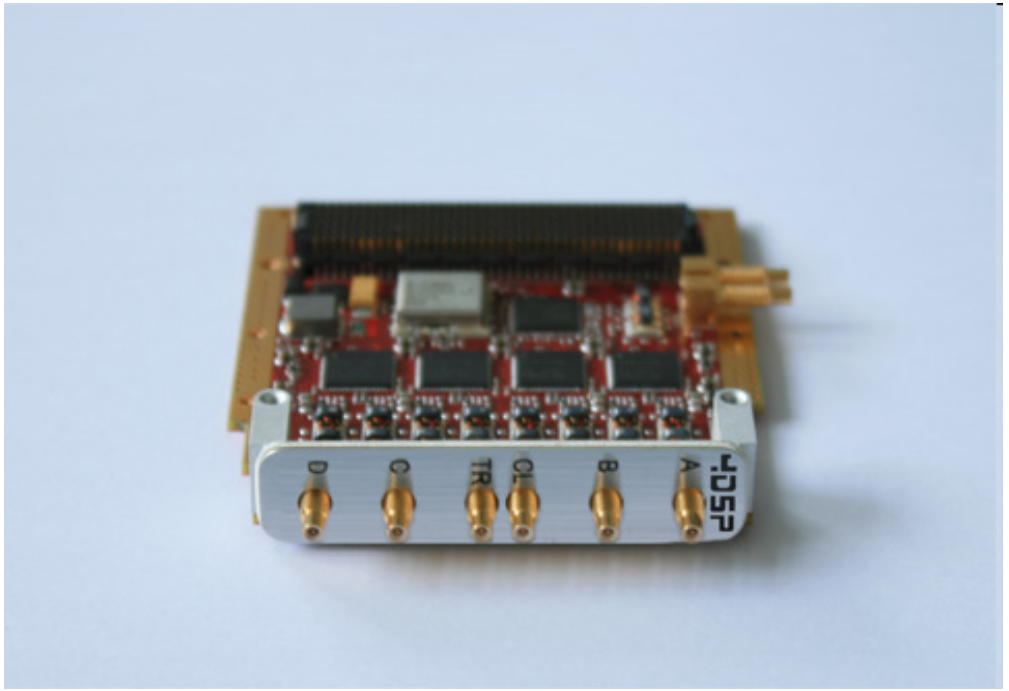
Why we chose FMC



- Well-specified standard
  - electrical interfaces, mechanical and thermal requirements
- Dedicated I2C lines for control
- Lots of commercial off-the-shelf ADC/DAC cards
- FMC-to-ZDOK+ adaptor for CASPER cards

4DSP FMC103

- 4 channel ADC
- 210MSPS
- 12-bit



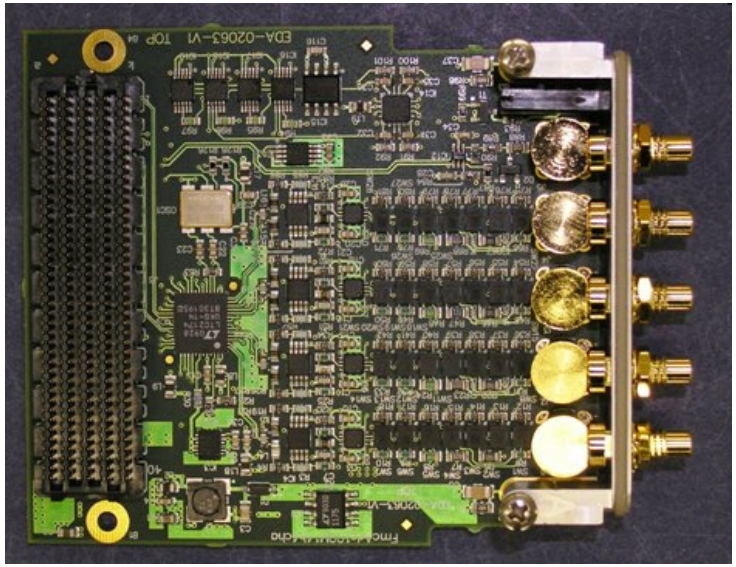
Curtis Wright ADC512

- Dual channel ADC
- 3 GSPS
- 8 bit



CERN FmcAdc100M14b4chb

- 4 channel ADC
- 105 MSPS
- 14 bit
- Open-hardware



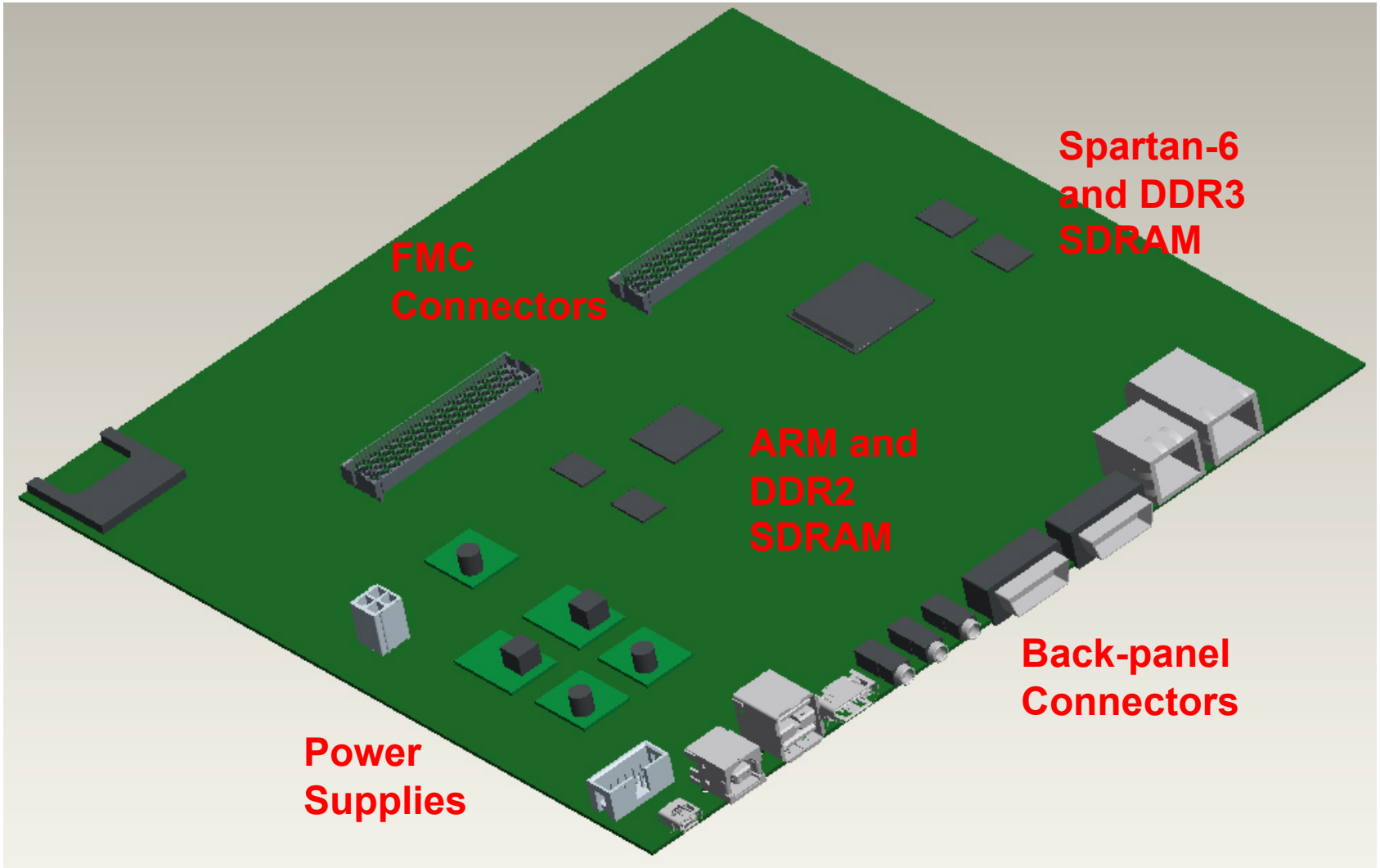
Optimise cost+performance



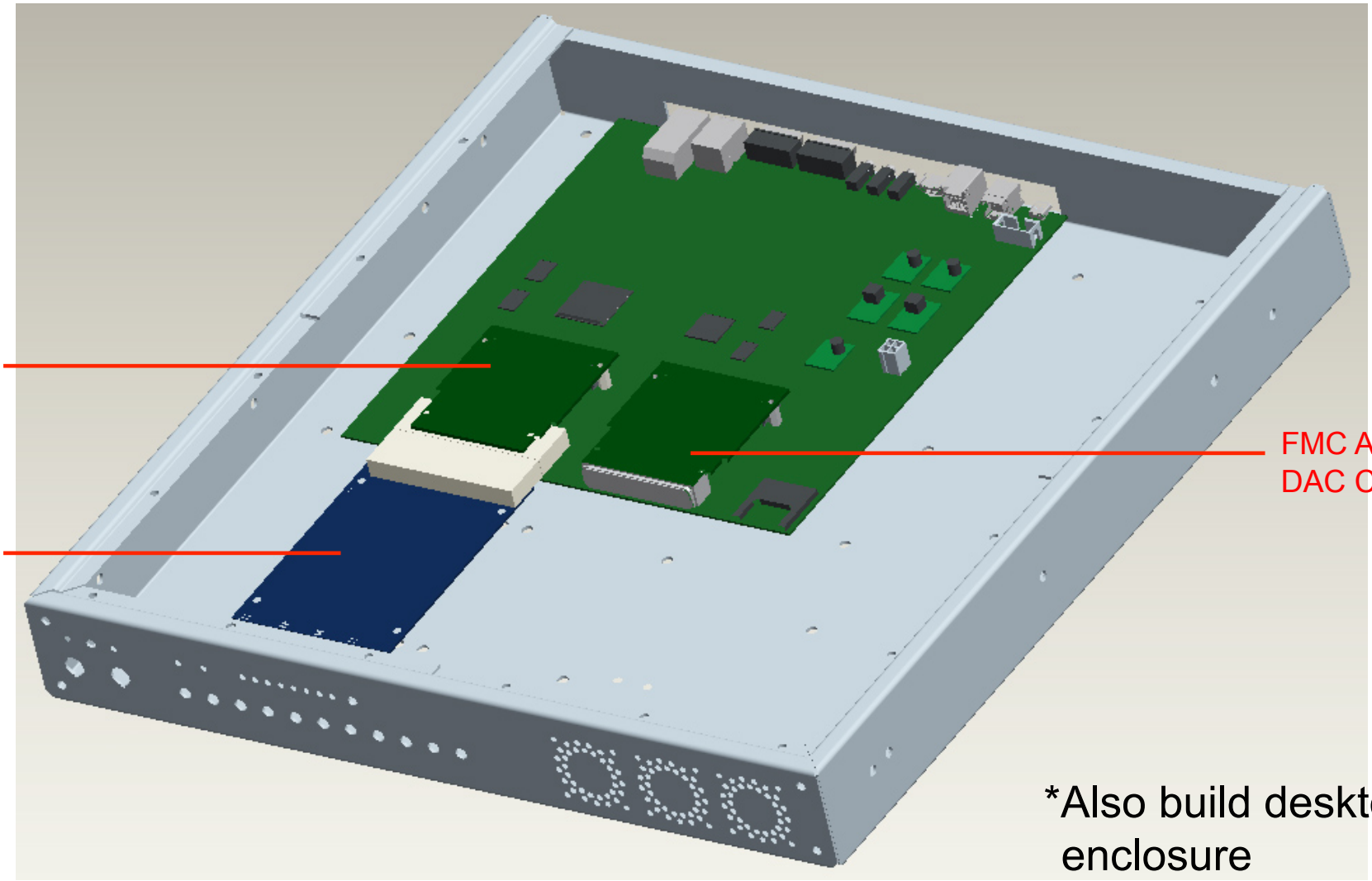
- Spartan-6 rather than Virtex-6
- 512MB DDR3, rather than QDR
- 2x 10Gbps links
- Total cost under $1500
- Training/research platform

The PCB

RHINO
Reconfigurable Hardware Interface for computatioN and radiO



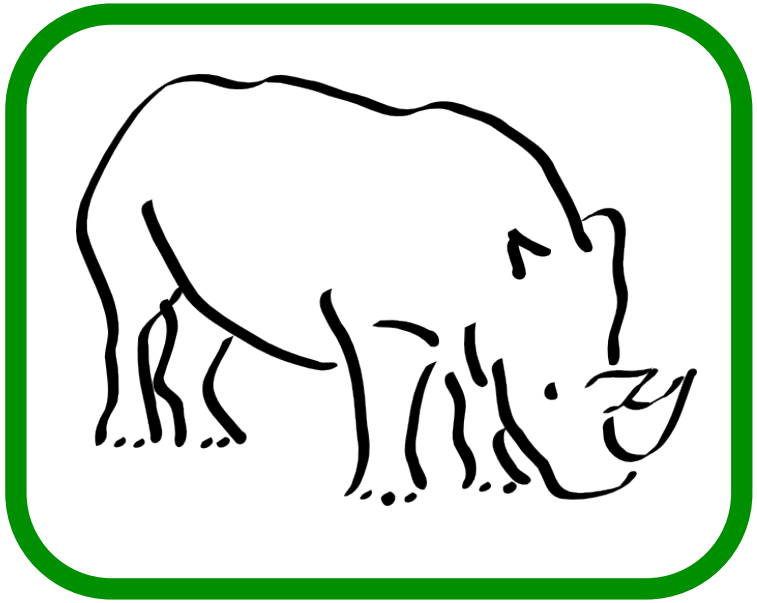
The Rhino Hide



*Also build desktop enclosure

Thank you

RHINO
Reconfigurable Hardware Interface for computatioN and radiO



http://rrsg2.ee.uct.ac.za/rhino