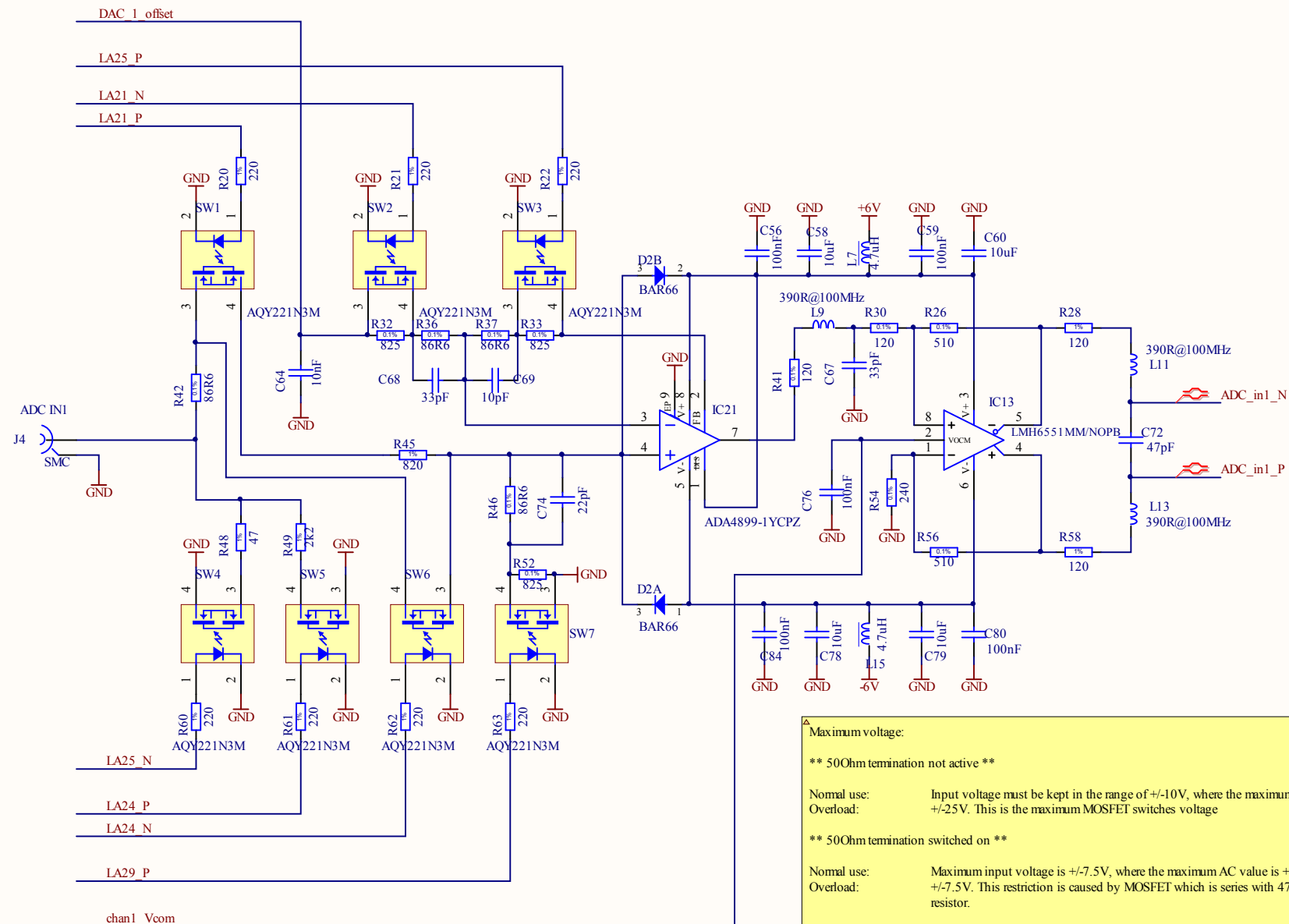




Maximum voltage:

** 50Ohm termination not active **

Normal use: Input voltage must be kept in the range of +/-10V, where the maximum AC value is +/-5V.
 Overload: +/-25V. This is the maximum MOSFET switches voltage

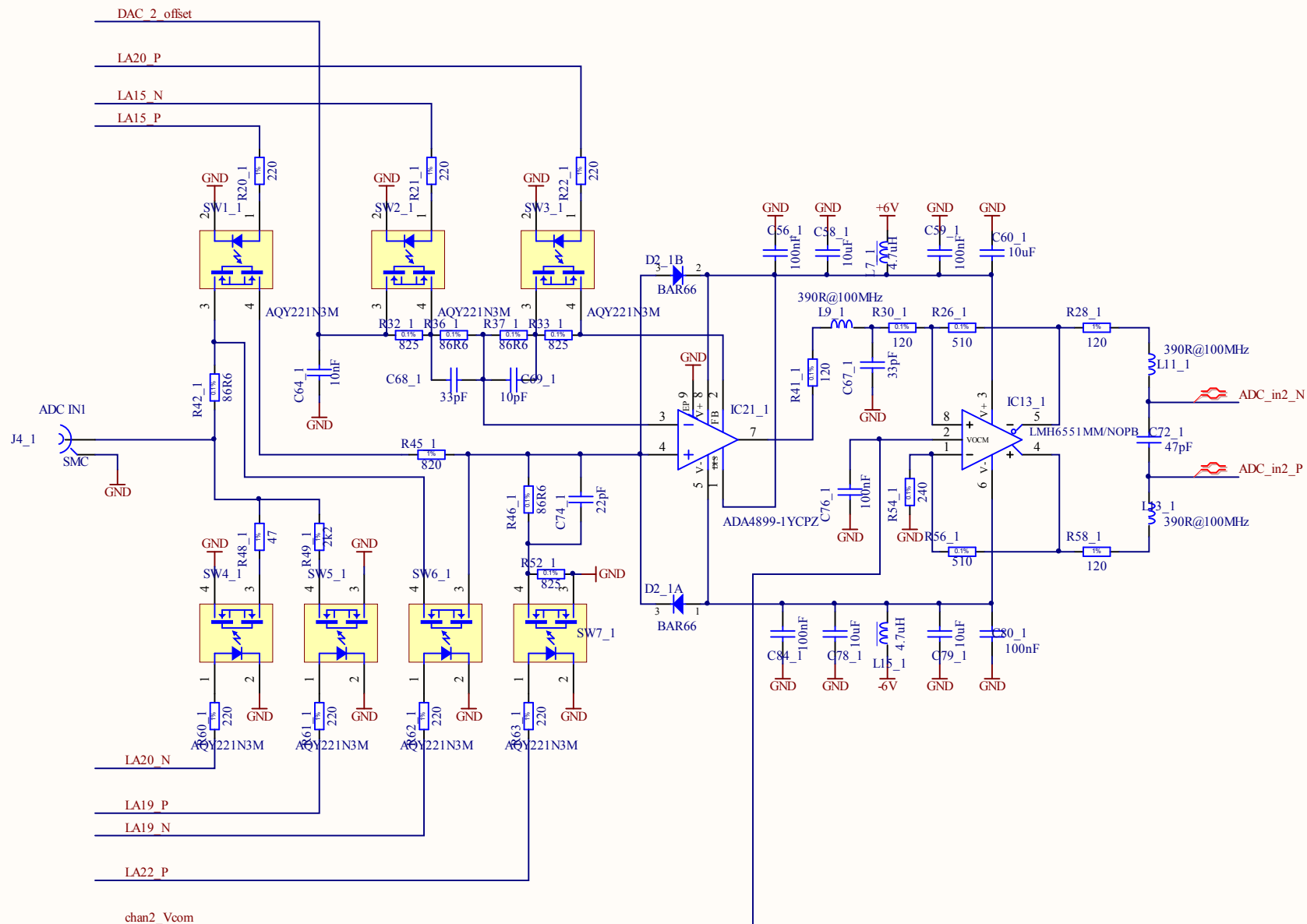
** 50Ohm termination switched on **

Normal use: Maximum input voltage is +/-7.5V, where the maximum AC value is +/-5V.
 Overload: +/-7.5V. This restriction is caused by MOSFET which is series with 470hm terminating resistor.

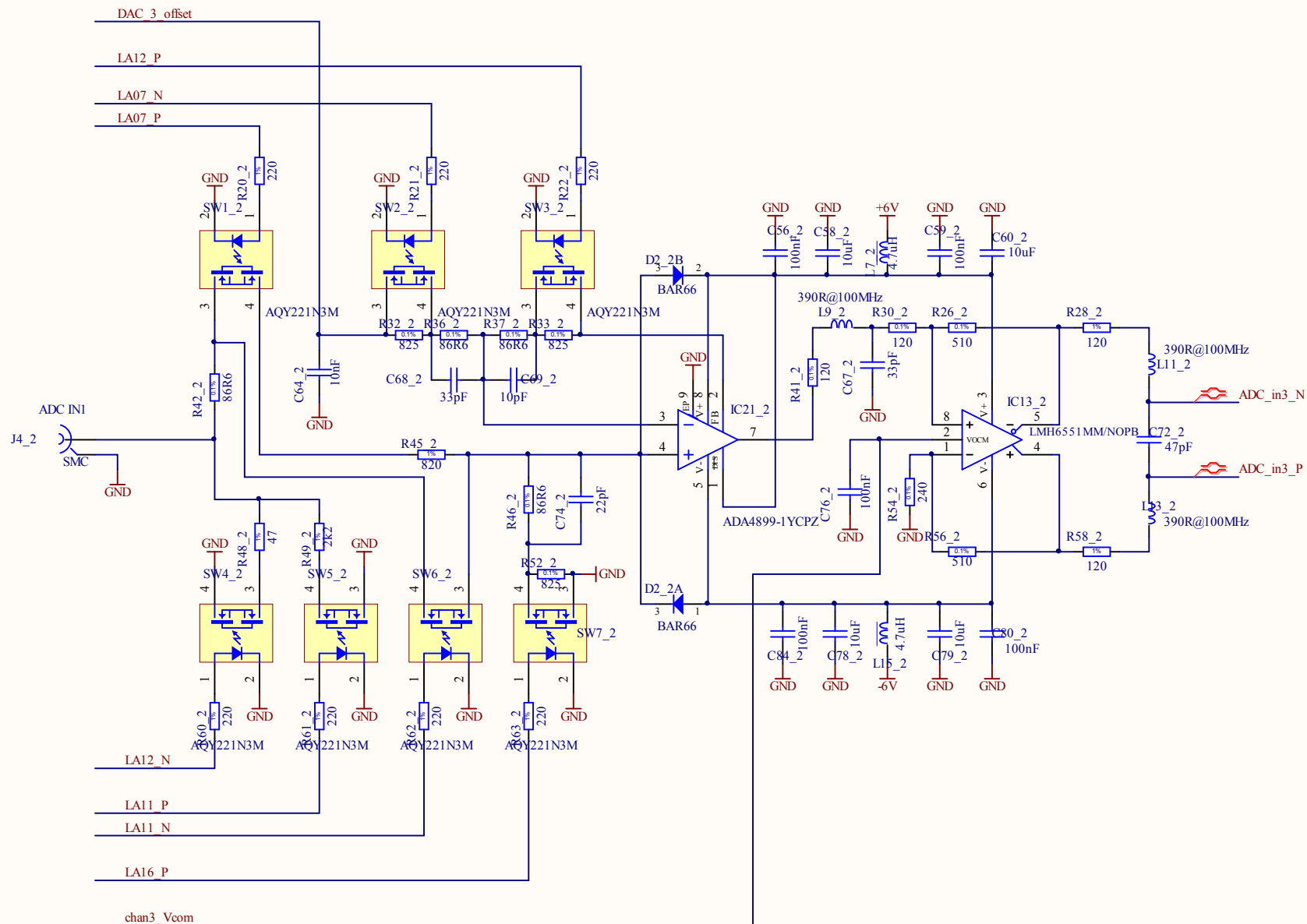
Overload may take only short time. Otherwise it may cause input resistors overheat even if input voltage or current

Project/Equipment		FmcAdc100M14b4cha	
Document		Designer	Designer
ENICE 	<i>Input stage 1</i>	Drawn by	Maciej Fimiarez
	<i>Amplifier and trigger receiver</i>	Check by	N.Lopez
		Last Mod.	-
		File	input_stage_1.SchDoc
		Print Date	08.03.2010 11:17:41
		Sheet	01 of 11
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02063-V1-0	
		Size	A4
		Rev	-

EDA-02063-V1-0



Project/Equipment		FmcAdc100M14b4cha	
Document		 Input stage 2 Amplifier and trigger receiver	
Designer	Designer	01/02/2010	
Drawn by	Maciej Fimiarz	-	
Check by	N.Lopez	08.03.2010	
Last Mod.	-	-	
File	input_stage_2.SchDoc		
Print Date	08.03.2010 11:17:41	Sheet	02 of 11
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02063-V1-0	See Rev
		A4	-

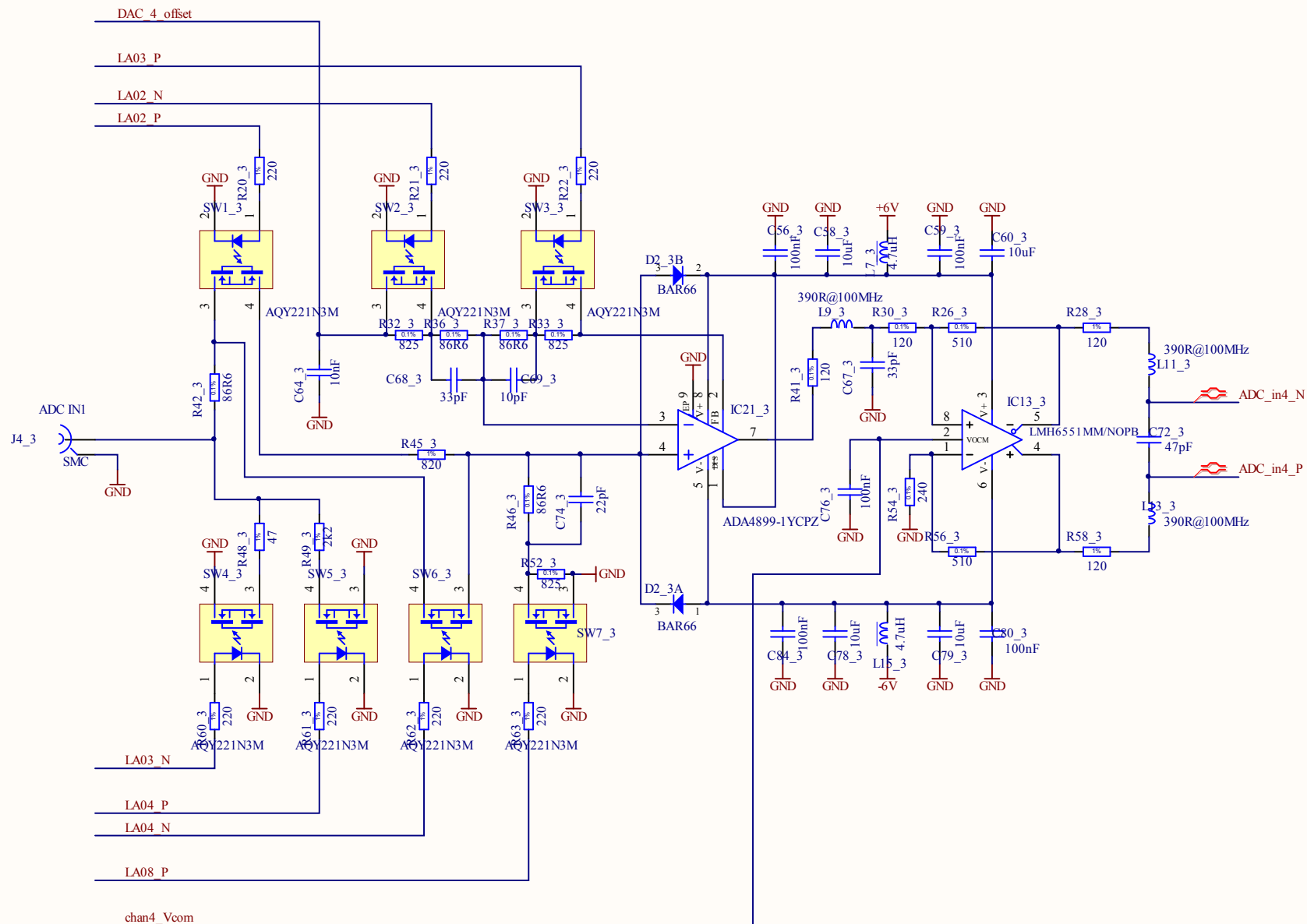


Project/Equipment		FmcAdc100M14b4cha	
Document		Designer Designer	
ENICE		Drawn by Maciej Fimiarz	01/02/2010
CERN		Check by N.Lopez	-
		Last Mod. -	08.03.2010
		File input_stage_3.SchDoc	
		Print Date 08.03.2010 11:17:42	Sheet 03 of 11
		Size A4	Rev -

Input stage 3 Amplifier and trigger receiver

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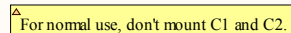


Project/Equipment		FmcAdc100M14b4cha	
Document		Designer Designer	
ENICE		Drawn by Maciej Fimiarez	01/02/2010
CERN		Check by N.Lopez	-
		Last Mod. -	08.03.2010
		File input_stage 4.SchDoc	
		Print Date 08.03.2010 11:17:42	Sheet 04 of 11
		Size A4	Rev -

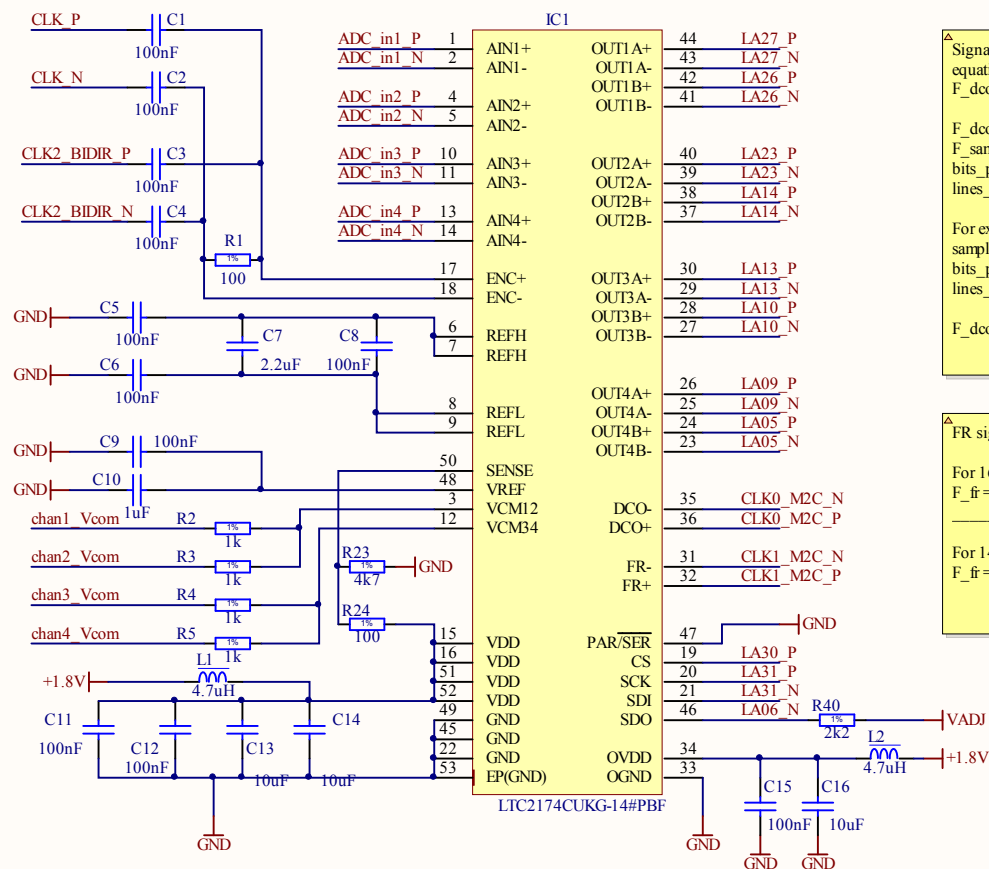
Input stage 4 Amplifier and trigger receiver

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EDA-02063-V1-0



For testing purpose remove C3 and C4 and solder C1 and C2. Clock needs to be delivered via not dedicated LA01 pair.



Signal frequency from DCO (CLK0_M2C) is given by following equation:

$$F_{dco} = F_{\text{sampling}} * \text{bits per sample} / \text{lines per channel} / 2$$

F_dco	- frequency of DCO signal
F_sampling	- ADC sampling frequency
bits_per_sample	- 14 (typical) or 16 (compatibility mode)
lines_per_channel	- 1 or 2 (typical) pairs for each channel

For example	
sampling freq.	- 100MSPs
bits_per_sample	- 14
lines per channel	- 2

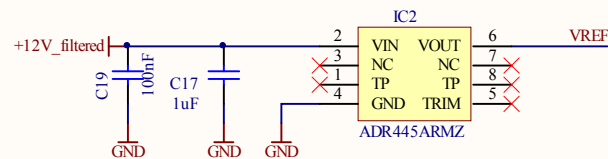
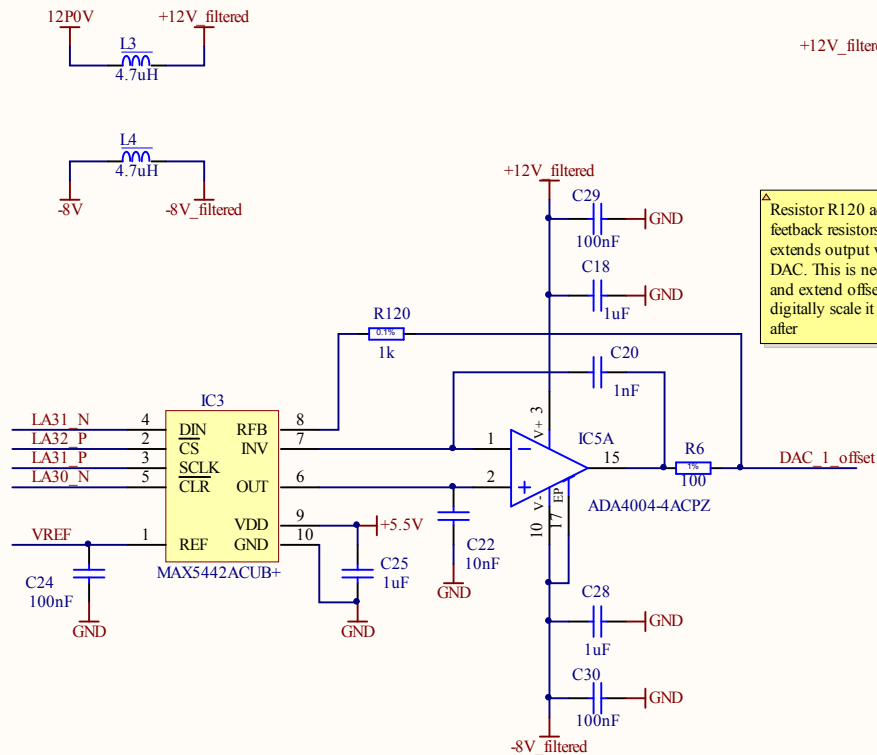
$$F_{\text{dco}} = 350\text{MHz}$$

△ FR signal frequency

For 16 bit output word length:
 $F_{fr} = F_{\text{sampling}}$

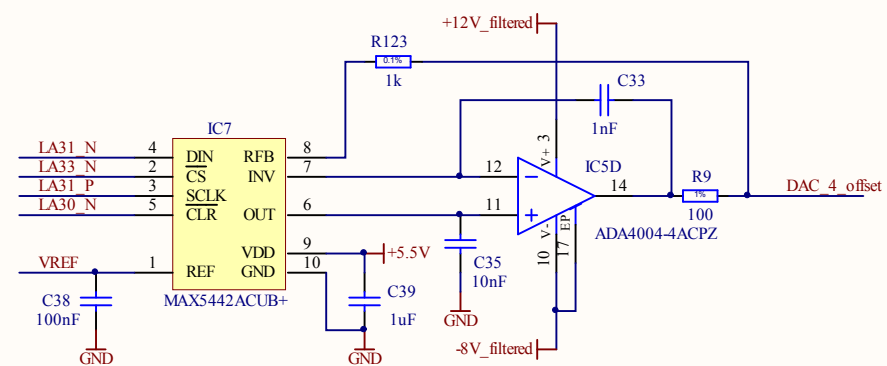
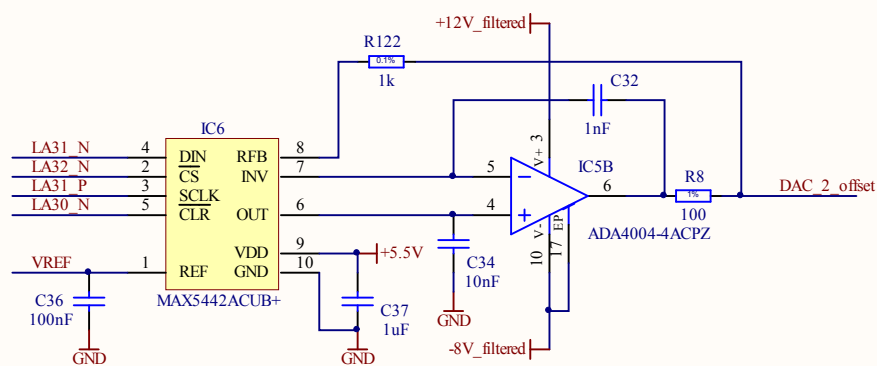
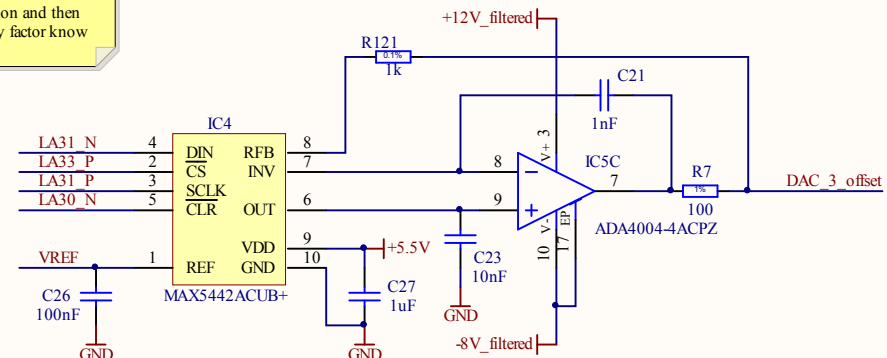
For 14 bit output word length:
 $F_{fr} = F_{sampling} / 2$

Project/Equipment		FmcAdc100M14b4cha	
Document		Designer	Designer
	Linear Technologies' ADC 105MSPS 14b	Drawn by	Maciej Fimiarczyk
		Check by	-
		Last Mod.	-
		File	ADC_SchDoc
		Print Date	08.03.2010 11:17:43
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Sheet	05 of 11
		EDA-02063-V1-0	Size A4 Rev



VREF is 5V.

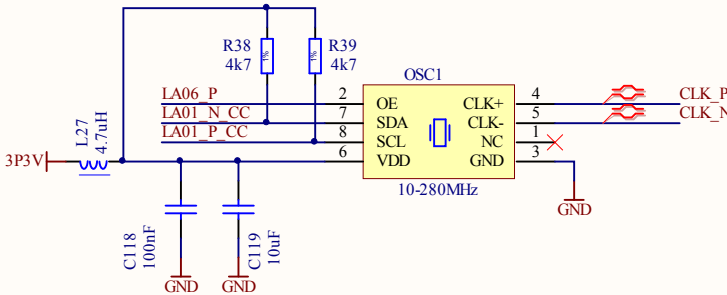
ADR445ARMZ must be replaced by ADR445BRZ. Second one has better thermal stability (3ppm/°C instead of 10ppm/°C)



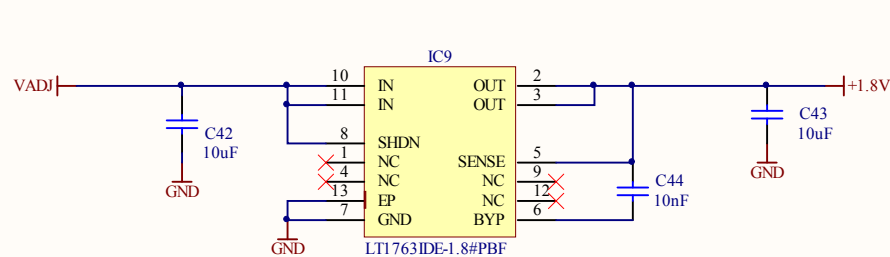
Project/Equipment		FmcAdc100M14b4cha	
Document		DACs and Vref source for offset correction	
	Designer	Designer	01/02/2010
	Drawn by	Maciej Fimiarz	-
	Check by	-	08.03.2010
	Last Mod.	-	-
	File	DAC.SchDoc	-
Print Date		08.03.2010 11:17:43	Sheet 06 of 11
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02063-V1-0	
		Size	Rev
		A4	-

Si570 is driven by separate I2C interface. It's because there is no possibility of externally setting the last significant bits of the base address (like in case of for example EEPROM memory). So, if two mezzanine cards are plugged to the carrier, conflict on I2C bus appears.

Base address: 0x55 - 1 0 1 0 1 0 1

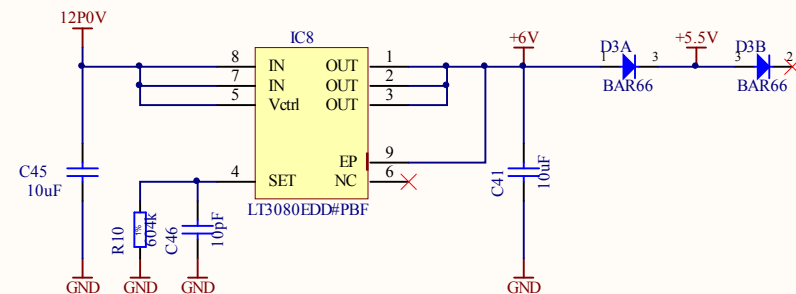


Project/Equipment		FmcAdc100M14b4cha		
Document		ADC clock generator		
	Designer	Designer		
	Drawn by	Maciej Fimiaryz	01/02/2010	
	Check by	-	-	
	Last Mod.	-	08.03.2010	
	File	clock_generator.SchDoc		
Print Date		08.03.2010 11:17:43	Sheet	08 of 11
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-02063-V1-0		Size A4 Rev -

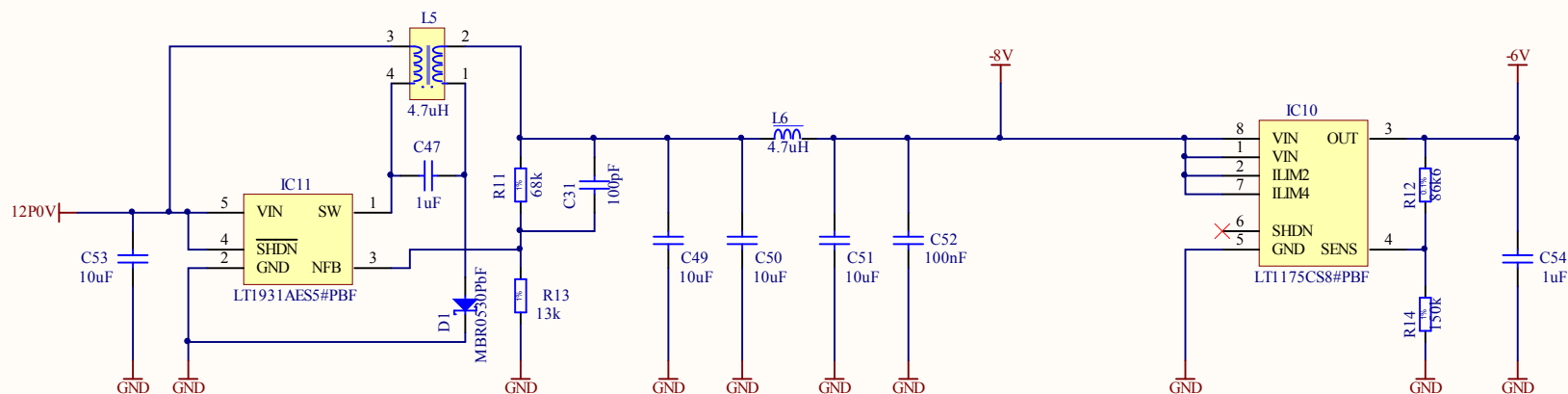


VADJ is set to 2.5V because:

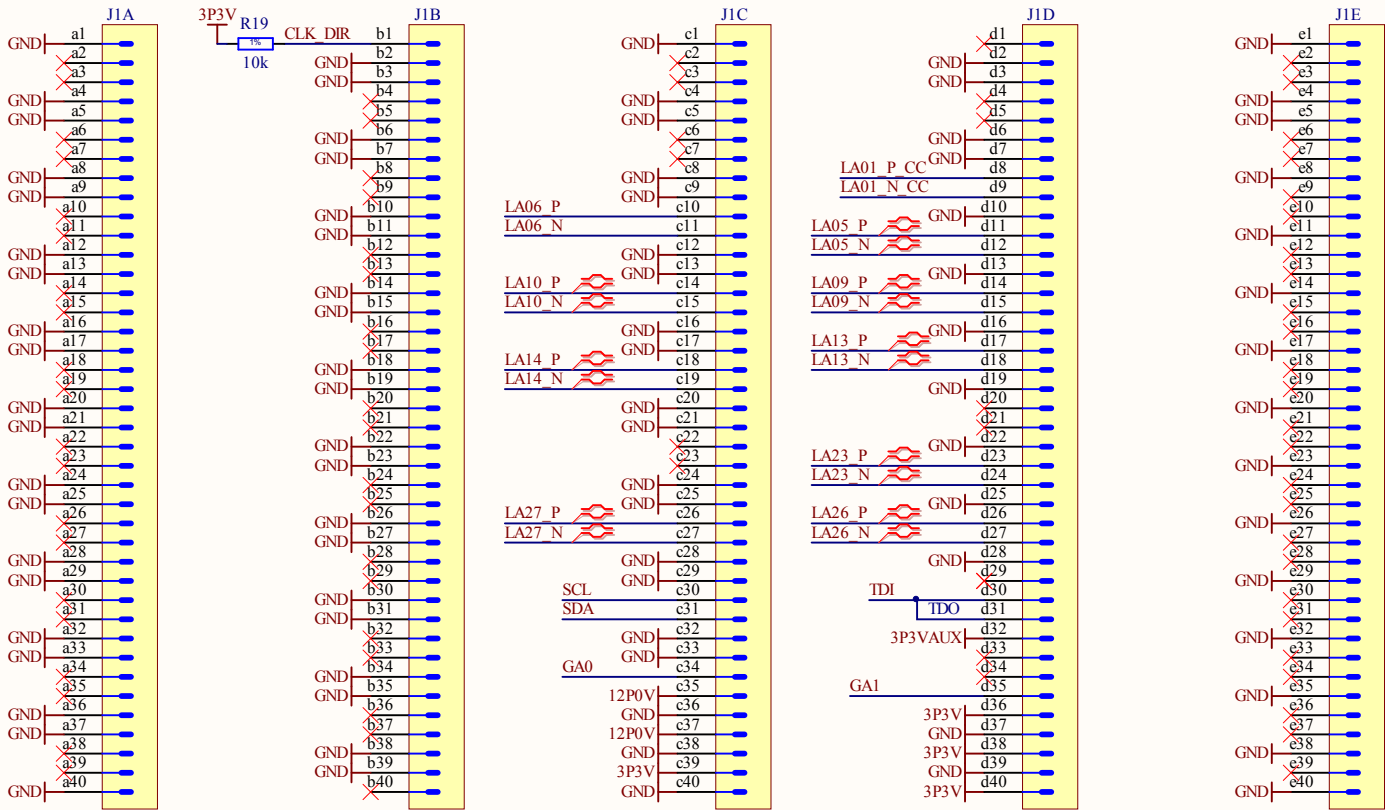
- there is no need of level matching for DAC SPI interface
- FMC board could be tested with Xilinx kit, where VADJ is fixed to 2.5V



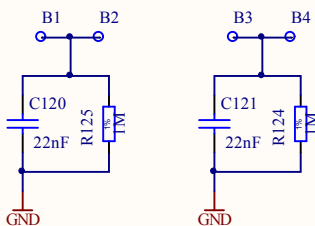
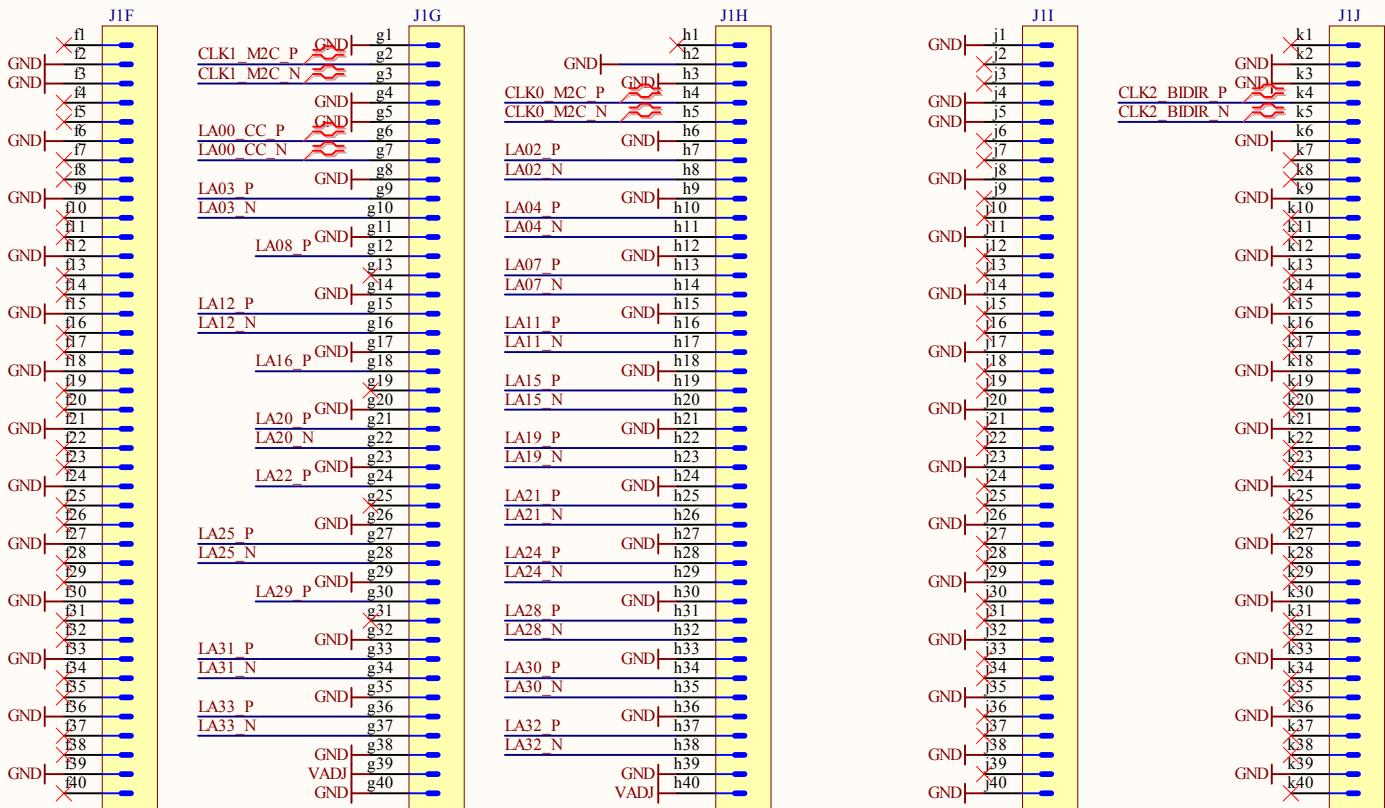
+5.5V is used as a power supply for offset creating DACs. The real value is 6V - 0.6... 0.7V which gives 5.3 ... 5.4V. It is lower than 5.5V - max. voltage for normal operation.



Project/Equipment		FmcAdc100M14b4cha	
Document		Power supplies	
	Designer	Designer	
	Drawn by	Maciej Fimiarz	01/02/2010
	Check by	-	-
	Last Mod.	-	08.03.2010
	File	power_supply.SchDoc	
Print Date		08.03.2010 11:17:44	Sheet 09 of 11
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CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.



B1 ... B4
screw holes for mounting the
FmcAdc to the carrier board.



FTG1 ... FTG6
Reference points for the
component mounting machine.

Project/Equipment	FmcAdc100M14b4cha		
Document	SAMTEC VITA 57 High Pin Count Connector		
ENICE	Designer	Designer	01/02/2010
CERN	Drawn by	Maciej Fimiarz	-
	Check by	N.Lopez	08.03.2010
	Last Mod.	-	08.03.2010
	File	SAMTEC connector.SchDoc	
	Print Date	08.03.2010 11:17:44	Sheet 10 of 11
	Size	A4	Rev -

Switches configuration:								
	channel 1	channel 2	channel 3	channel 4				
sw1	LA21_P	LA15_P	LA07_P	LA02_P				
sw2	LA21_N	LA15_N	LA07_N	LA02_N				
sw3	LA25_P	LA20_P	LA12_P	LA03_P				
sw4	LA25_N	LA20_N	LA12_N	LA03_N				
sw5	LA24_P	LA19_P	LA11_P	LA04_P				
sw6	LA24_N	LA19_N	LA11_N	LA04_N				
sw7	LA29_P	LA22_P	LA16_P	LA08_P				
		sw1	sw2	sw3	sw4	sw5	sw6	sw7
100mV range:		on	on	off	-	off	on	off
1V range:		on	off	off	-	on	off	off
10V range:		on	off	on	-	off	off	on
DC offset error calibration:		off	off	off	off	off	off	on
50Ohm termination:		-	-	-	on	-	-	-

SPI - SCK	LA31_P
SPI - DIN	LA31_N
SPI - DAC_RST	LA30_N
SPI - CS_ADC	LA30_P
SPI - CS_DAC1	LA32_P
SPI - CS_DAC2	LA32_N
SPI - CS_DAC3	LA33_P
SPI - CS_DAC4	LA33_N
SPI - SDO_ADC	LA06_N
LED_TOP	LA28_P
LED_BOT	LA28_N
Clock generator enable	LA06_P
Clock generator I2C - SCL	LA01_P_CC
Clock generator I2C - SDA	LA01_N_CC
Lines left unconnected:	
LA08_N, LA16_N, LA22_N, LA29_N, LA17_P_CC, LA17_N_CC, LA18_P_CC, LA18_N_CC	

Trigger:	LA00_P_CC	LA00_N_CC
DCO - output clock	CLK0_M2C_P	CLK0_M2C_N
FR - frame sync	CLK1_M2C_P	CLK1_M2C_N
ADC clock	CLK2_BIDIR_P	CLK2_BIDIR_N
ADC output 1 A	LA27_P	LA27_N
ADC output 1 B	LA26_P	LA26_N
ADC output 2 A	LA23_P	LA23_N
ADC output 2 B	LA14_P	LA14_N
ADC output 3 A	LA13_P	LA13_N
ADC output 3 B	LA10_P	LA10_N
ADC output 4 A	LA09_P	LA09_N
ADC output 4 B	LA05_P	LA05_N

Project/Equipment		FmcAdc100M14b4cha		
Document				
	Designer		Designer	
	Drawn by		Maciej Fimiarez	01/02/2010
	Check by		-	-
	Last Mod.		-	08.03.2010
	File		pin_configuration.SchDoc	
Print Date		08.03.2010	11:17:44	Sheet 11 of 11
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