

Project/Equipment FmcAdc100M14b4cha

Document



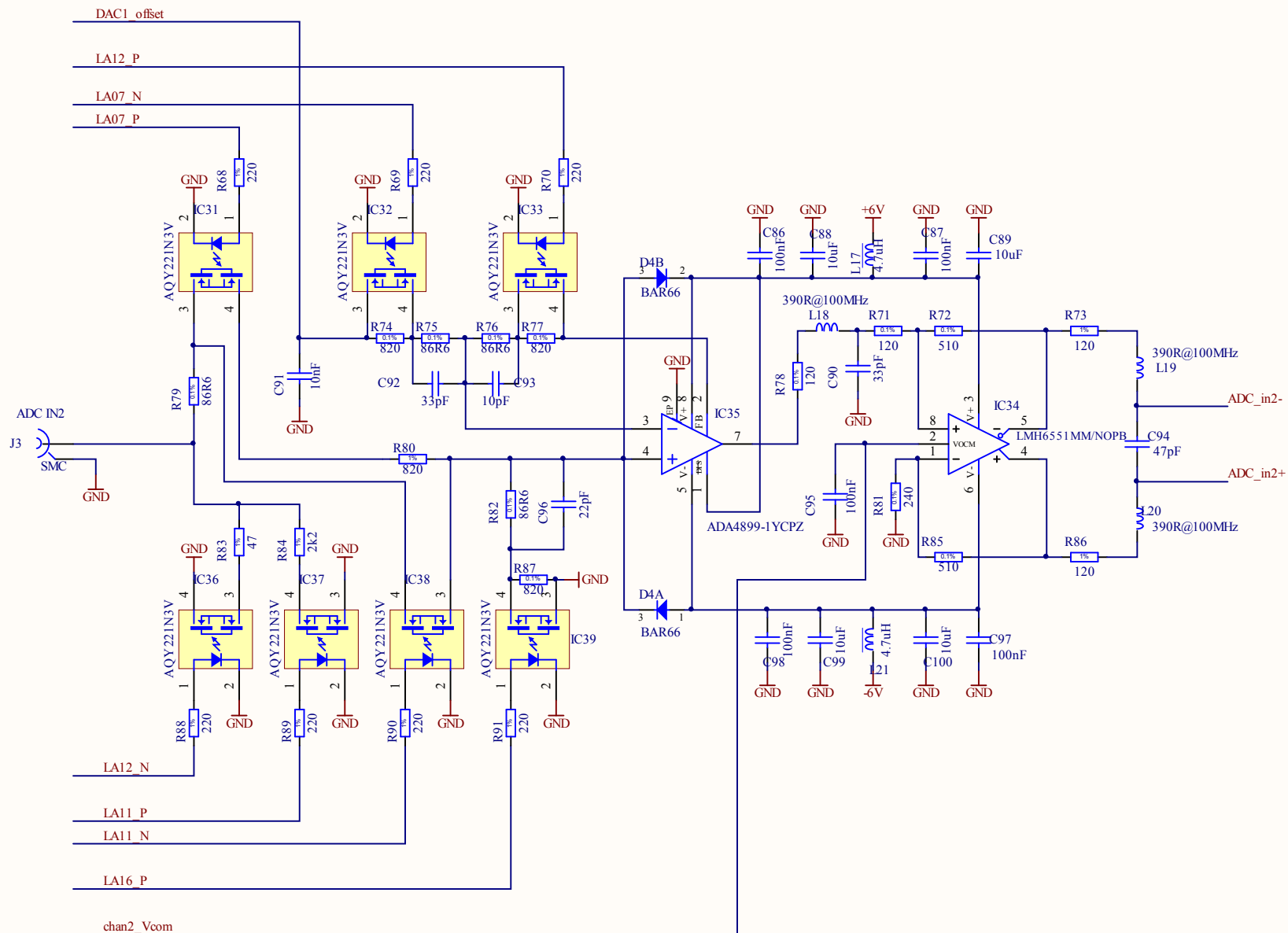
SAMTEC VITA 57 **High Pin Count Connector**

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CH-1211 Genève 23 - Switzerland

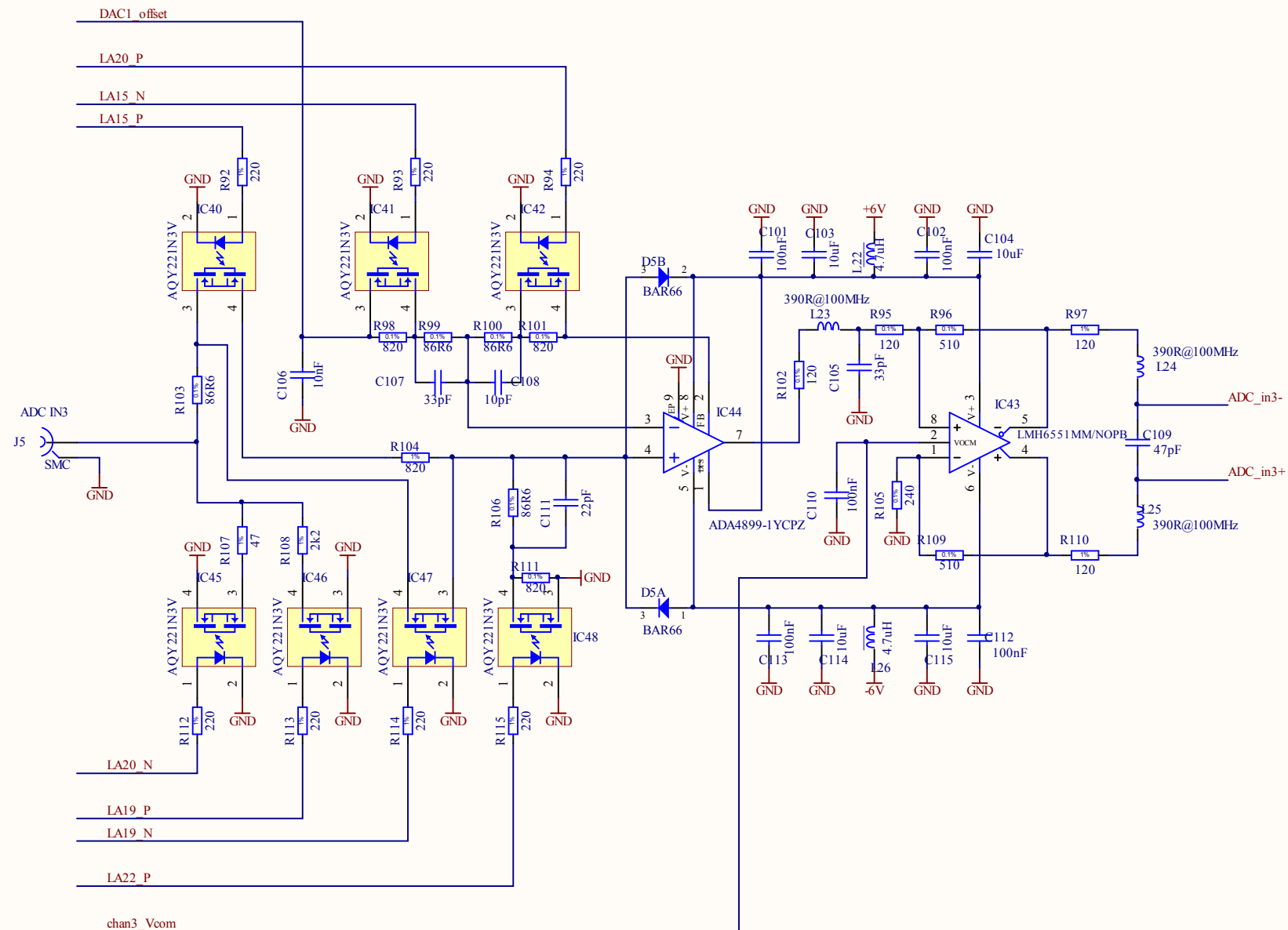
Designer	Designer	
Drawn by	Maciej Fimiarz	01/02/2010
Check by	N.Lopez	-
Last Mod.		03.02.2010
File	SAMTEC connector.SchDoc	
Print Date	04.02.2010 09:09:58	Sheet 1 of 10

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Size A4 Rev -

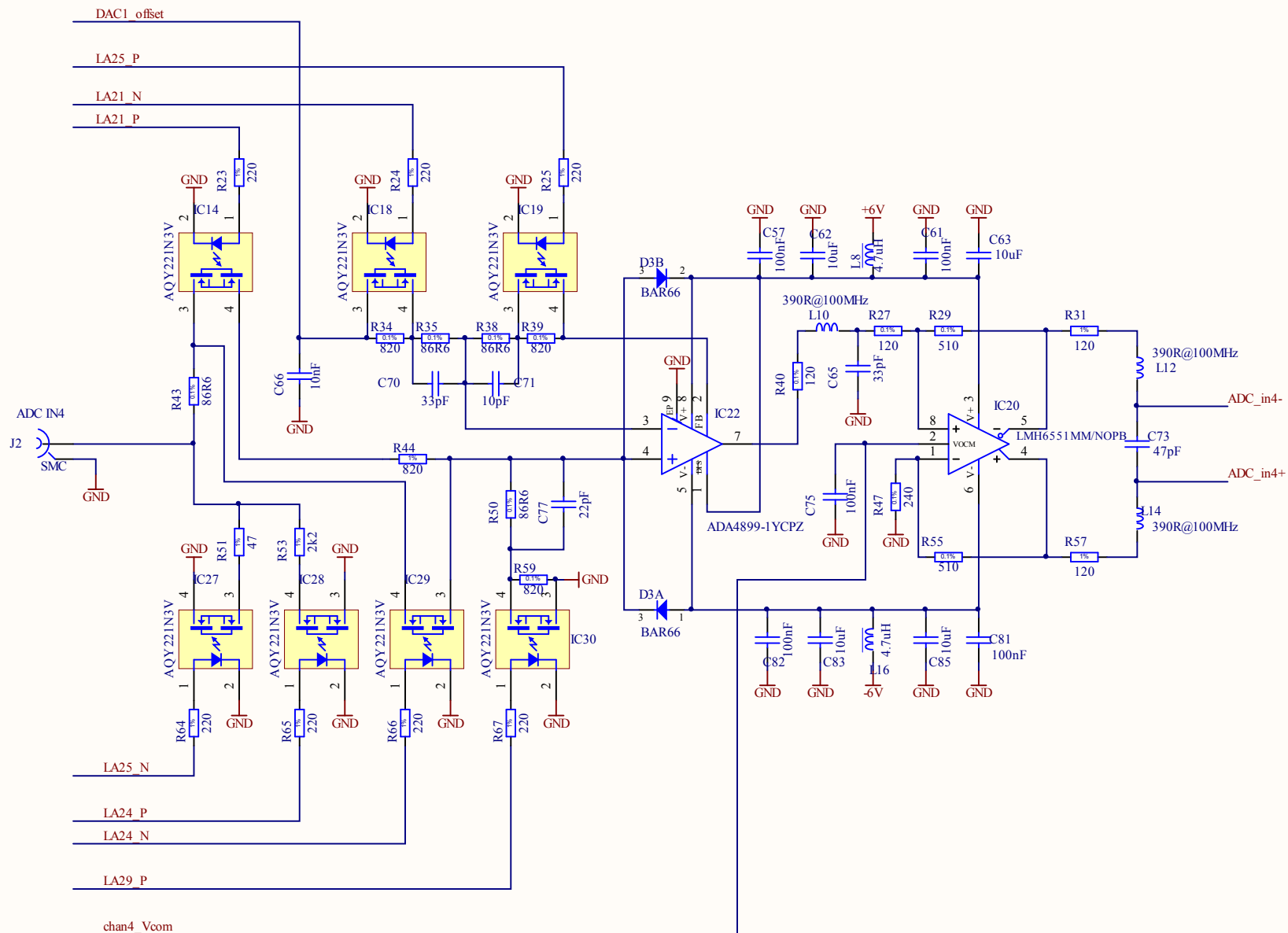


Project/Equipment		FmcAdc100M14b4cha	
Document		Designer Designer Drawn by Maciej Fimiarz 01/02/2010 Check by - - Last Mod. - 04.02.2010 File input_stage 2.SchDoc Print Date 04.02.2010 09:09:59 Sheet 3 of 10	
ENICE CERN		Input stage 2 Amplifier and trigger receiver European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	
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Project/Equipment		FmcAdc100M14b4cha	
Document		Input stage 3 Amplifier and trigger receiver	
Designer	Designer	01/02/2010	
Drawn by	Maciej Fimiarz	-	
Check by	-	04.02.2010	
Last Mod.	-	-	
File	input_stage_3.SchDoc	Sheet	4 of 10
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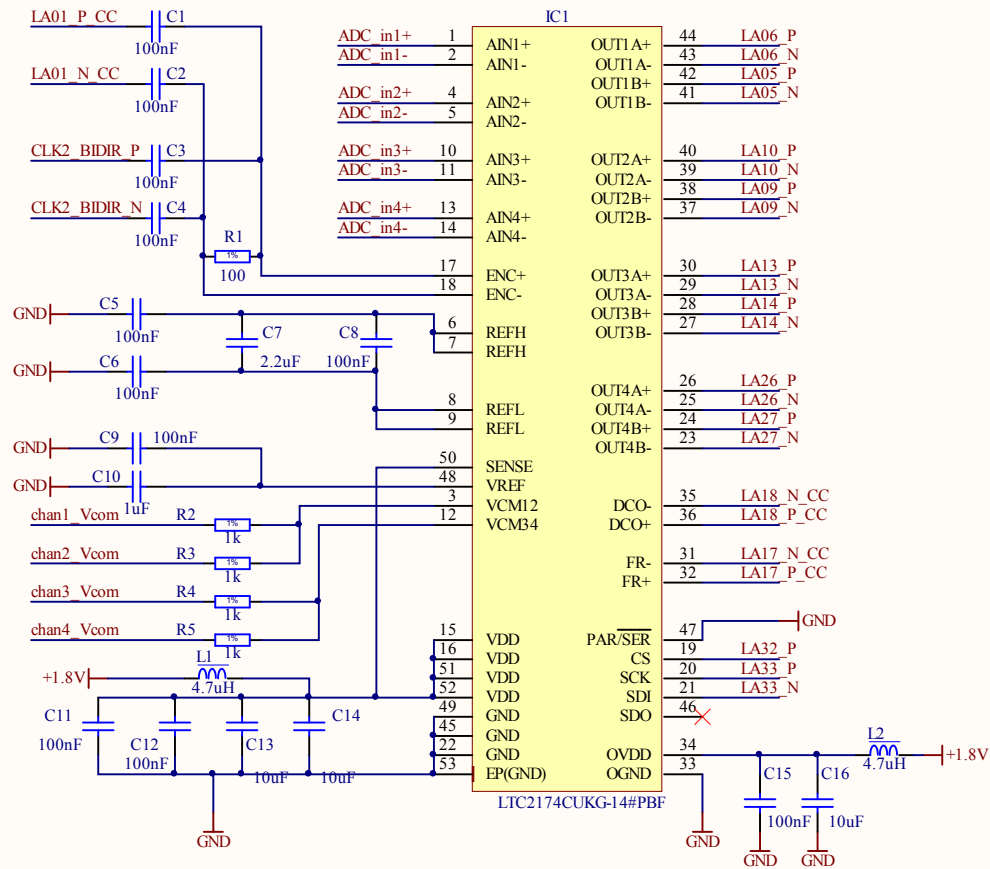
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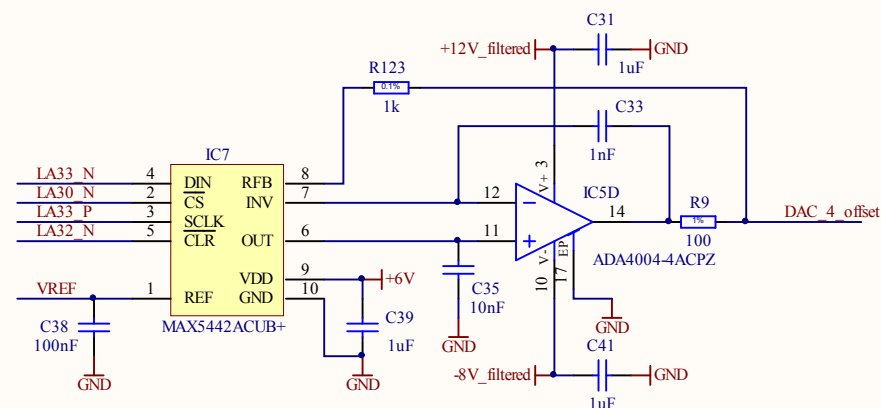
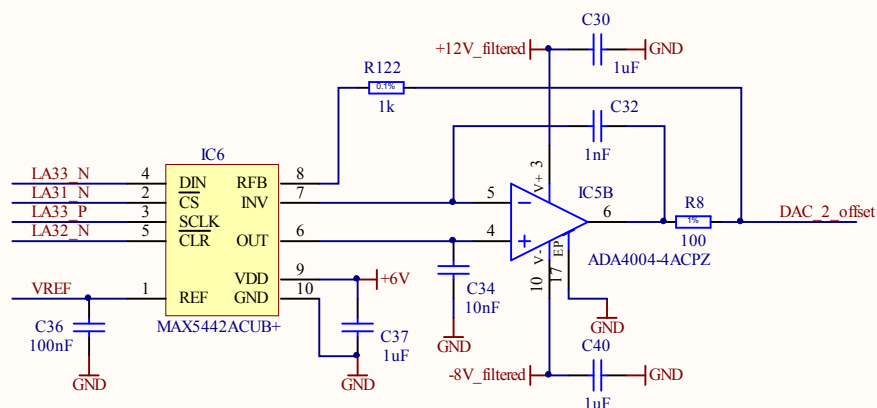
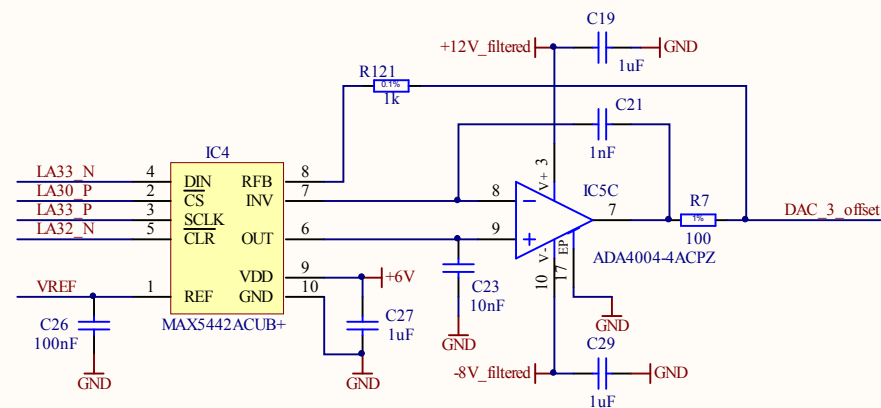
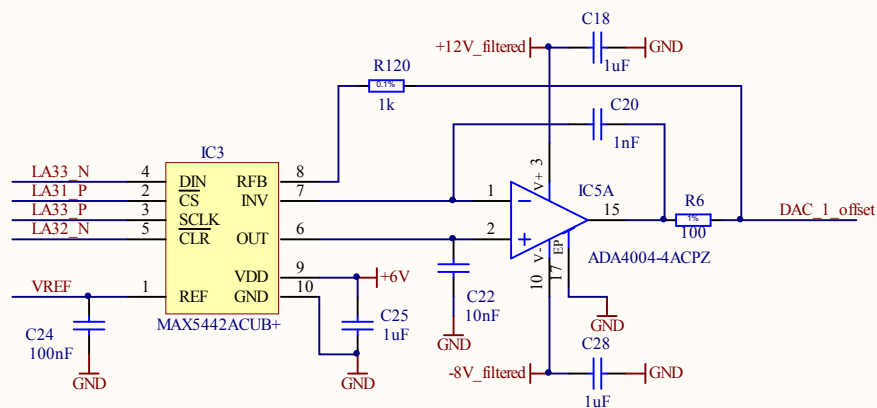
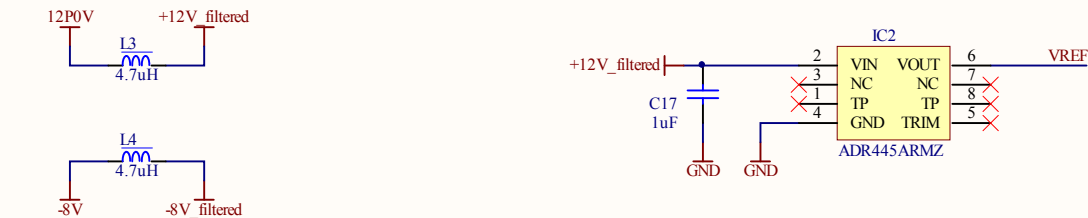
Project/Equipment		FmcAdc100M14b4cha	
Document		ENICE CERN Input stage 4 Amplifier and trigger receiver	
Designer		Designer	
Drawn by		Maciej Fimiarz	01/02/2010
Check by		-	-
Last Mod.		-	04.02.2010
File		input_stage_4.SchDoc	
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For normal use, don't mount C1 and C2.

For testing purpose remove C3 and C4 and solder C1 and C2. Clock needs to be delivered via not dedicated LA01 pair.



Project/Equipment		FmcAdc100M14b4cha	
Document		Designer Designer	
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		Check by	-
		Last Mod.	04.02.2010
		File	ADC.SchDoc
		Print Date	04.02.2010 09:10:00
		Sheet	6 of 10
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Project/Equipment		FmcAdc100M14b4cha	
Document		Designer Designer	
ENICE		Drawn by Maciej Fimiarz	
CERN		Check by -	
		Last Mod. -	
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		Sheet 7 of 10	
		Size A4	
		Rev -	

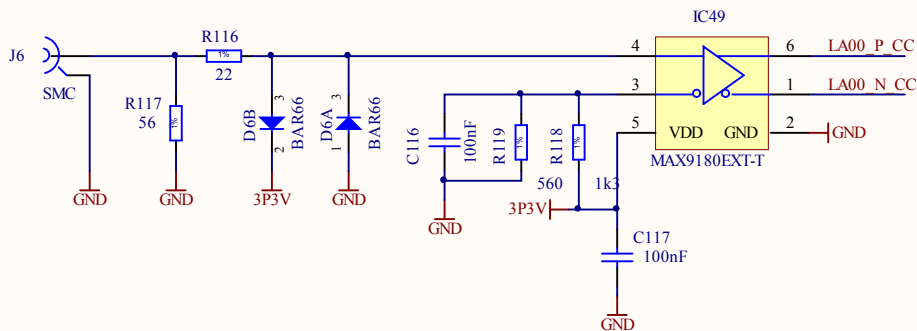
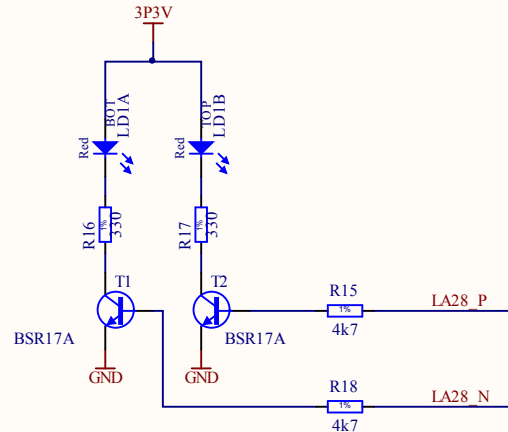
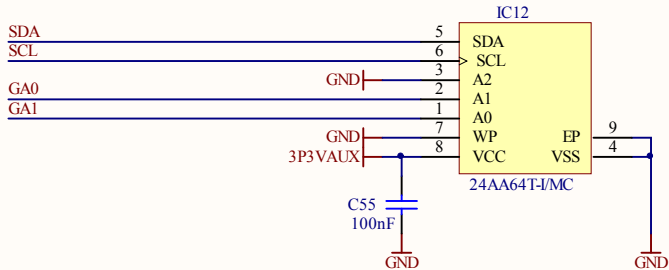
**DACs and Vref source
for offset correction**

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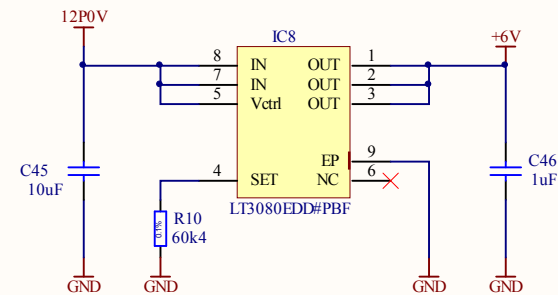
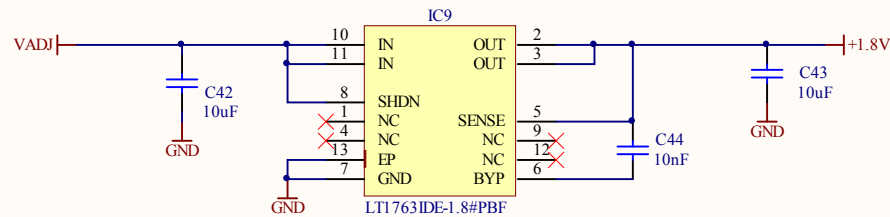
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Warning!
Following the VITA 57.1 standard:
GA0 goes to A1
GA1 goes to A0

24AA64T A6-A3 = 1010
MCP9801 A6-A3 = 1001

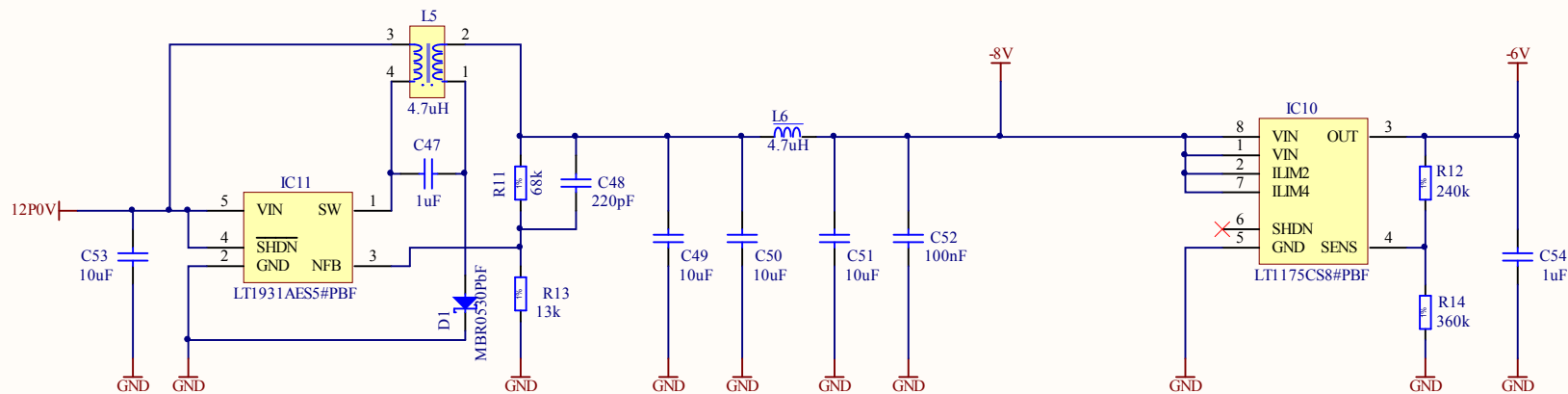


Project/Equipment		FmcAdc100M14b4cha	
Document		Designer Designer	
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		File	I2C_mem_LED.SchDoc
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Print Date	04.02.2010 09:10:00
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VADJ is set to 2.5V because:

- there is no need of level matching for DAC SPI interface
- FMC board could be tested with Xilinx kit, where VADJ is fixed to 2.5V



Project/Equipment		FmcAdc100M14b4cha		
Document		Power supplies		
	Designer	Designer	01/02/2010	
	Drawn by	Maciej Fimiarz	-	
	Check by	-	04.02.2010	
	Last Mod.	-	-	
	File	power_supply.SchDoc	-	
Print Date		04.02.2010 09:10:00	Sheet	9 of 10
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Switches configuration:								
	channel 1	channel 2	channel 3	channel 4				
sw1	LA02_P	LA07_P	LA15_P	LA21_P				
sw2	LA02_N	LA07_N	LA15_N	LA21_N				
sw3	LA03_P	LA12_P	LA20_P	LA25_P				
sw4	LA03_N	LA12_N	LA20_N	LA25_N				
sw5	LA04_P	LA11_P	LA19_P	LA24_P				
sw6	LA04_N	LA11_N	LA19_N	LA24_N				
sw7	LA08_P	LA16_P	LA22_P	LA29_P				
		sw1	sw2	sw3	sw4	sw5	sw6	sw7
100mV range:		on	on	off	-	off	on	off
1V range:		on	off	off	-	on	off	off
10V range:		on	off	on	-	off	off	on
DC offset error calibration:		off	off	off	off	off	off	on
50Ohm termination:		-	-	-	on	-	-	-

SPI - SCK	LA33_P
SPI - DIN	LA33_N
SPI - DAC_RST	LA32_N
SPI - CS_ADC	LA32_P
SPI - CS_DAC1	LA31_P
SPI - CS_DAC2	LA31_N
SPI - CS_DAC3	LA30_P
SPI - CS_DAC4	LA30_N
LED1	LA28_P
LED2	LA28_N

Trigger:	LA00_P_CC	LA00_N_CC	these lines can be swapped
DCO - output clock	LA18_P_CC	LA18_N_CC	
FR - frame sync	LA17_P_CC	LA17_N_CC	
optional ADC clock	LA01_P_CC	LA01_N_CC	
ADC clock	CLK2_BIDIR_P	CLK2_BIDIR_N	
ADC output 1 A	LA06_P	LA06_N	
ADC output 1 B	LA05_P	LA05_N	
ADC output 2 A	LA10_P	LA10_N	
ADC output 2 B	LA09_P	LA09_N	
ADC output 3 A	LA13_P	LA13_N	
ADC output 3 B	LA14_P	LA14_N	
ADC output 4 A	LA26_P	LA26_N	
ADC output 4 B	LA27_P	LA27_N	

Every single pair can be swapped with another to make routing simpler.

Every single line can be swapped with another without any restriction.