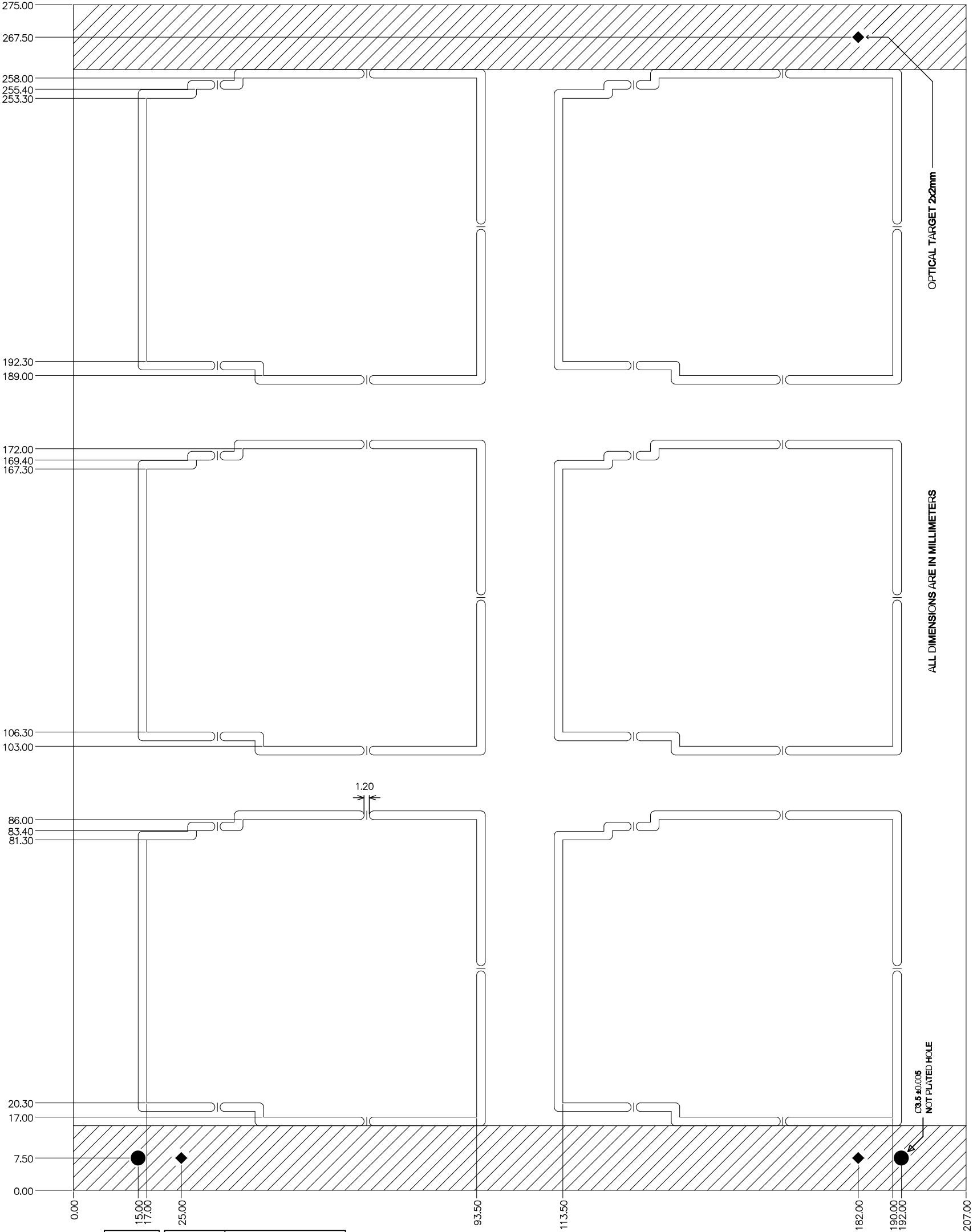
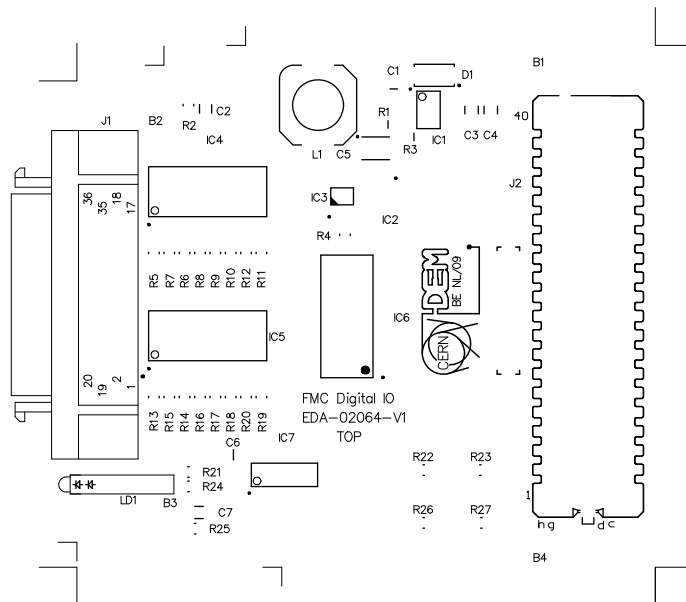




Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

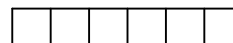
Print Date 13.01.2010 13:46:55

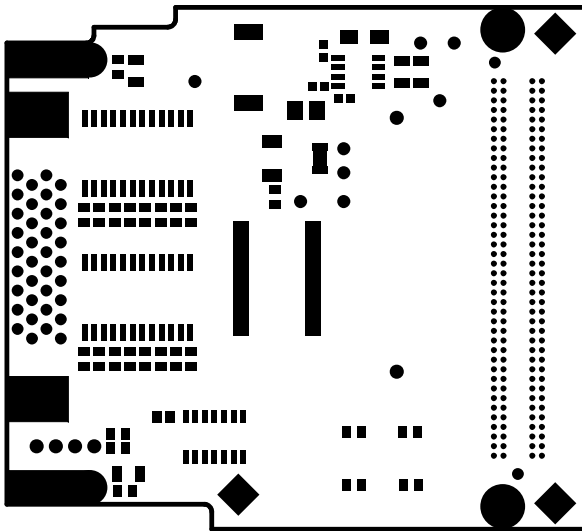


Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:54

Top Overlay

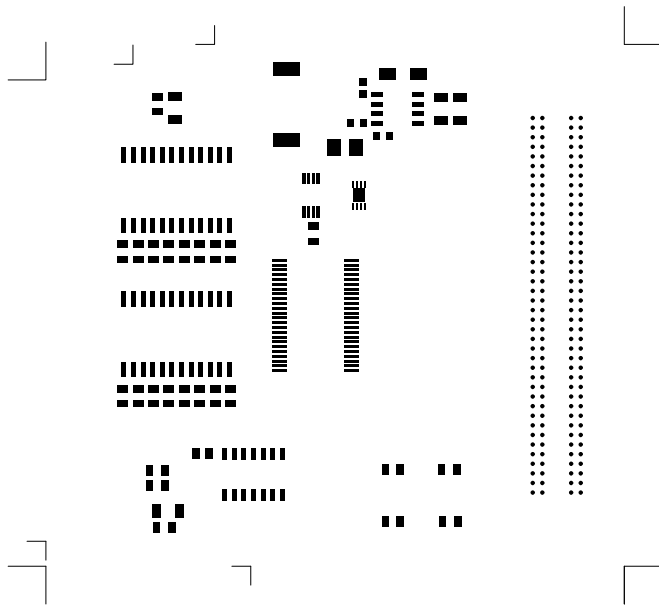




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Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

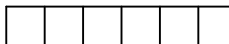
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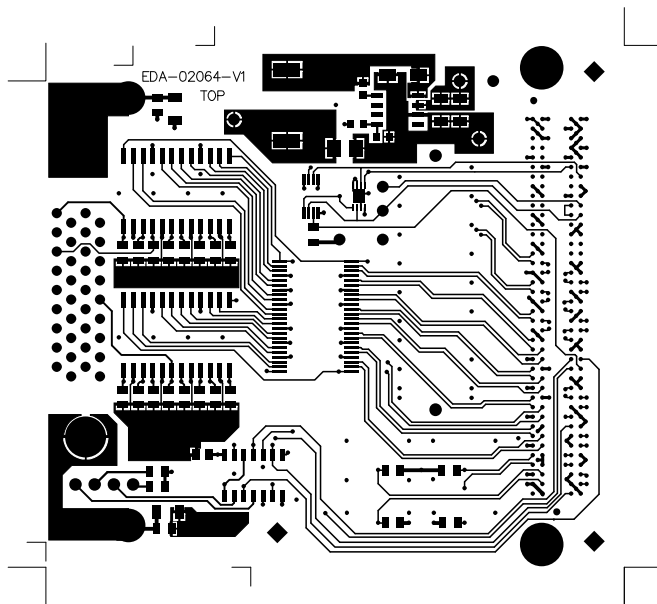
Top Solder



Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-
Print Date	13.01.2010 13:46:54

Top Paste



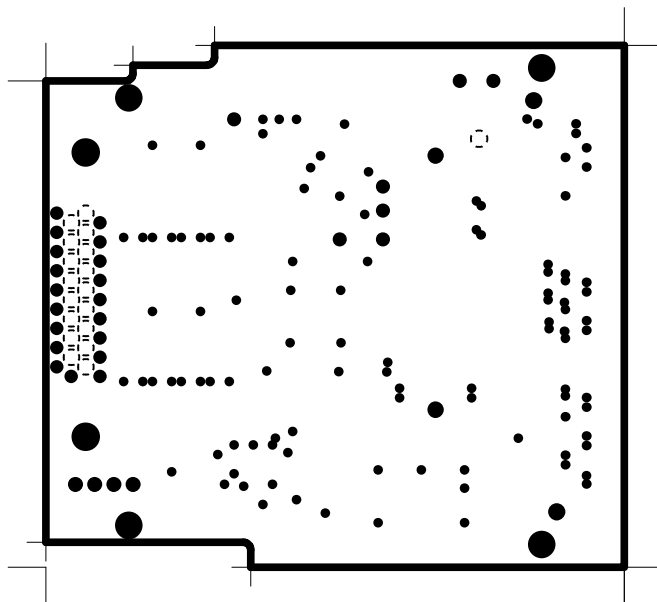


Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:53

Top Layer

1					
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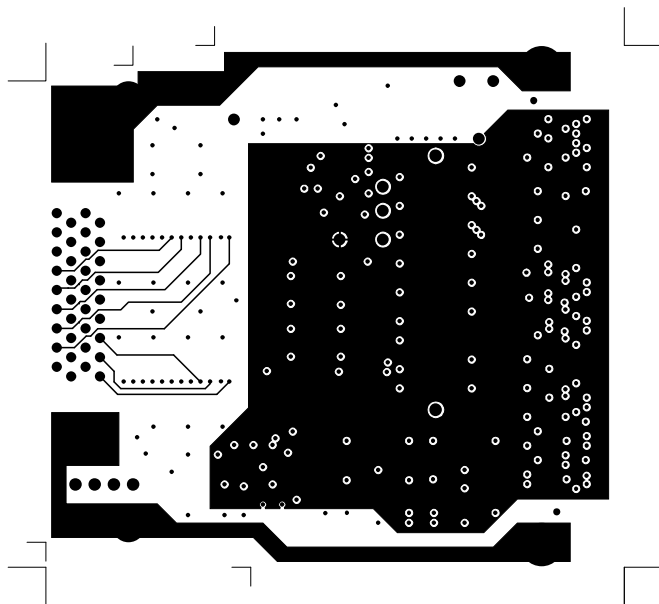


Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:53

plane 15 GND

2

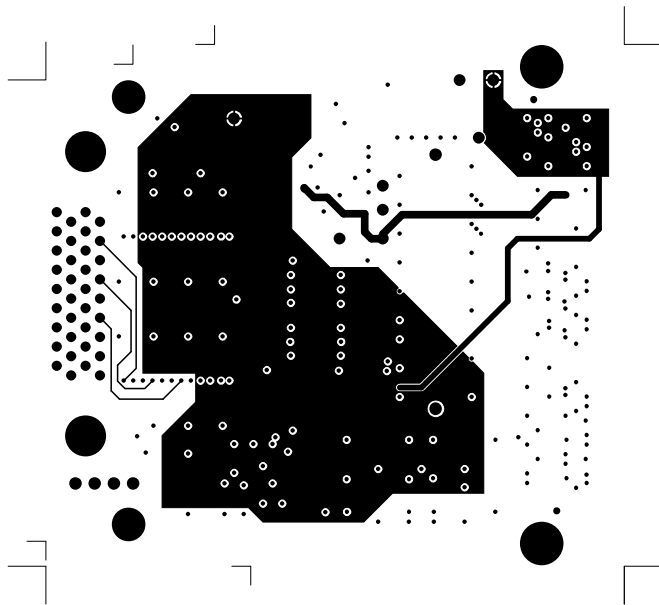


Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:53

L3 VADU.signals

		3			
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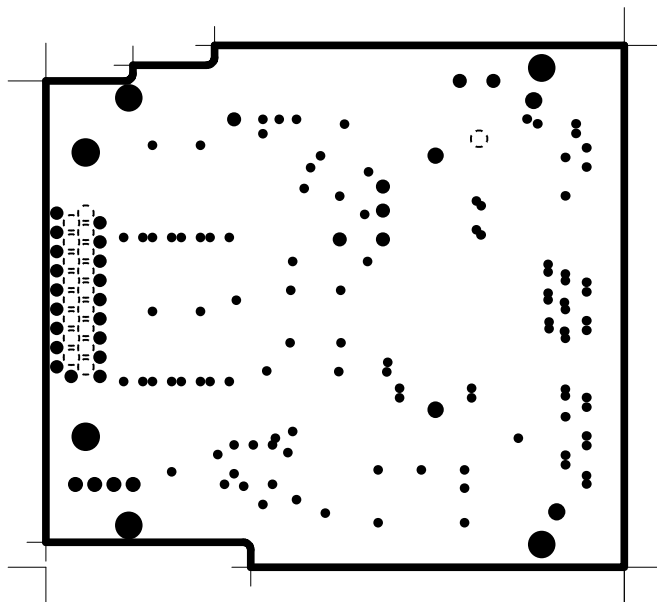


Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:54

17 2b01 3b21 3b21V01X 1b01 4J

			4		
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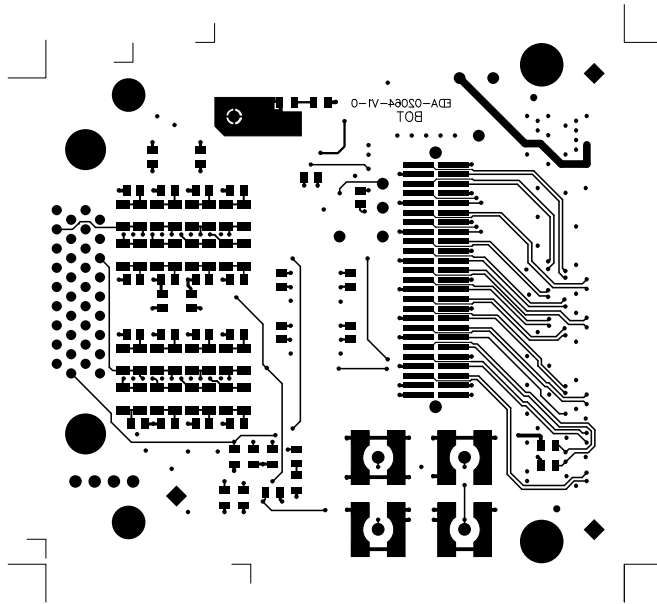


Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:54

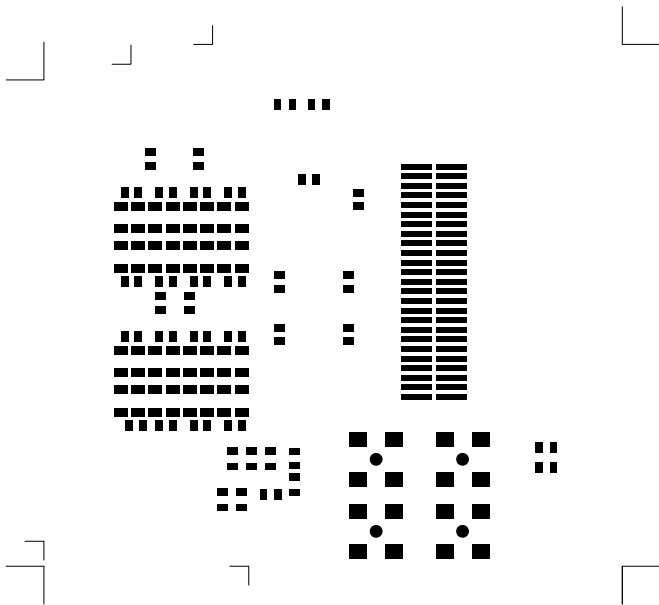
Plane L5 GND

5



Number	EDA-02064-V1
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DATE	07-12-2009
MOD.	-

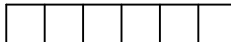
Print Date 13.01.2010 13:46:54

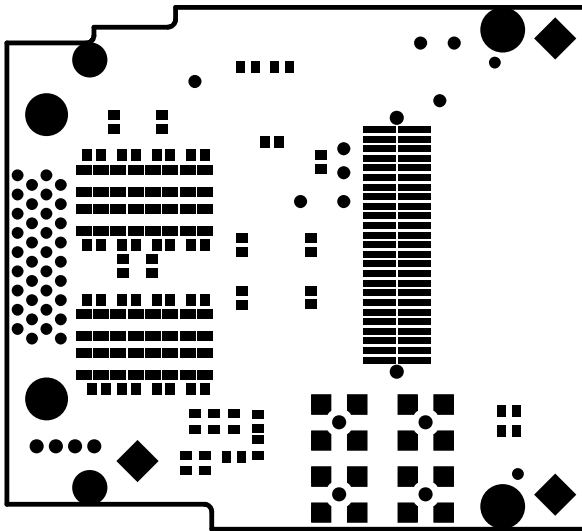


Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:54

Bottom Paste





Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:55

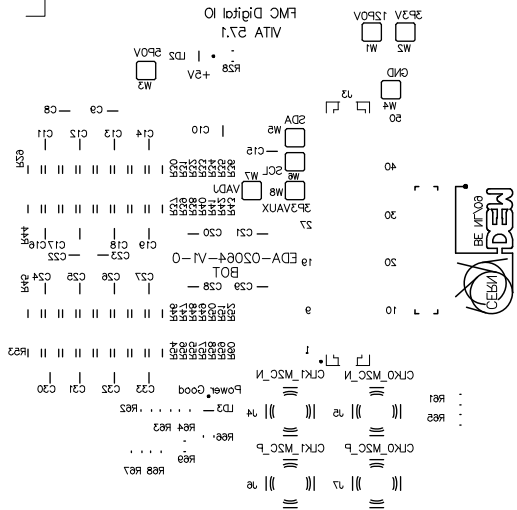
Bottom Solder

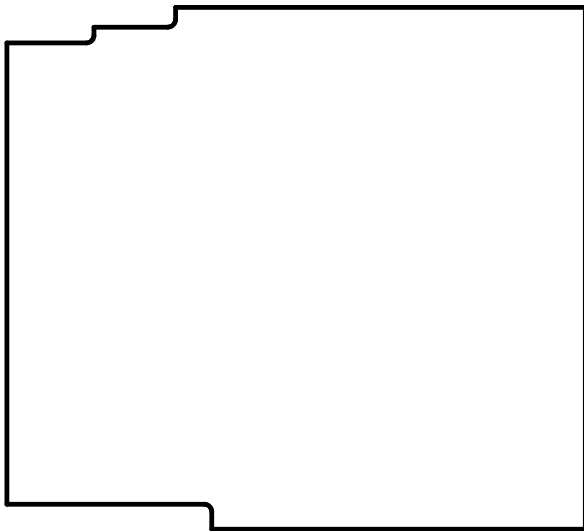


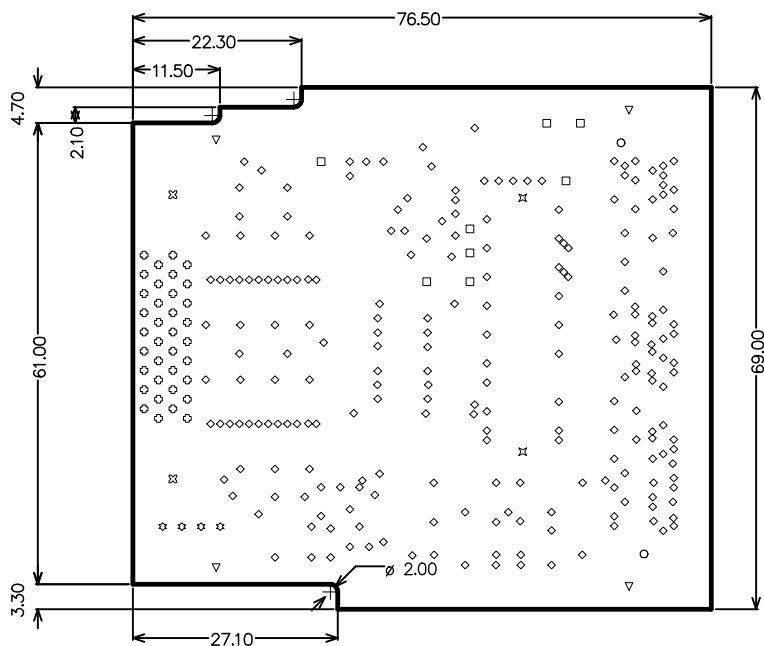
Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	-

Print Date 13.01.2010 13:46:54

Bottom Overlay







Symbol	Hit Count	Tool Size	Plated	Hole Type
◇	229	11.811mil (0.3mm)	PTH	Round
◊	36	31.496mil (0.8mm)	PTH	Round
□	8	35.433mil (0.9mm)	PTH	Round
✱	4	39.37mil (1mm)	PTH	Round
✱	2	47.244mil (1.2mm)	NPTH	Round
○	2	51.181mil (1.3mm)	NPTH	Round
▽	4	106.299mil (2.7mm)	PTH	Round
⊗	2	110.236mil (2.8mm)	PTH	Round
287 Total				

Layer Stack Up Detail for: EDA-02064-V1_pcb.PcbDoc

LAYER IDENTIFICATION		LINE WIDTH	FINISHED COPPER THICKNESS	CONTROLLED IMPEDANCE +/-10%	DIELECTRIC THICKNESS *=CRITICAL
TOP LAYER	SIGNAL LAYER	0.224mm	35 um	50 Ohms	* 0.150mm
LAYER 2	GND PLANE	—	35 um	xx Ohms	0.5mm
LAYER 3	PWR Signals	—	35 um	xx Ohms	0.150mm
LAYER 4	PWR Signals	—	35 um	xx Ohms	0.5mm
LAYER 5	GND PLANE	—	35 um	xx Ohms	* 0.150mm
BOTTOM LAYER	SIGNAL LAYER	0.224mm	35 um	50 Ohms	1.6mm
FINISHED BOARD THICKNESS +/-10%					



Number	EDA-02064-V1
Drawn By	CEGELEC NL
DATE	07-12-2009
MOD.	—

Print Date 13.01.2010 13:46:55

Components 139
Pins 643
Vias 229
Holes 287
Nets 133