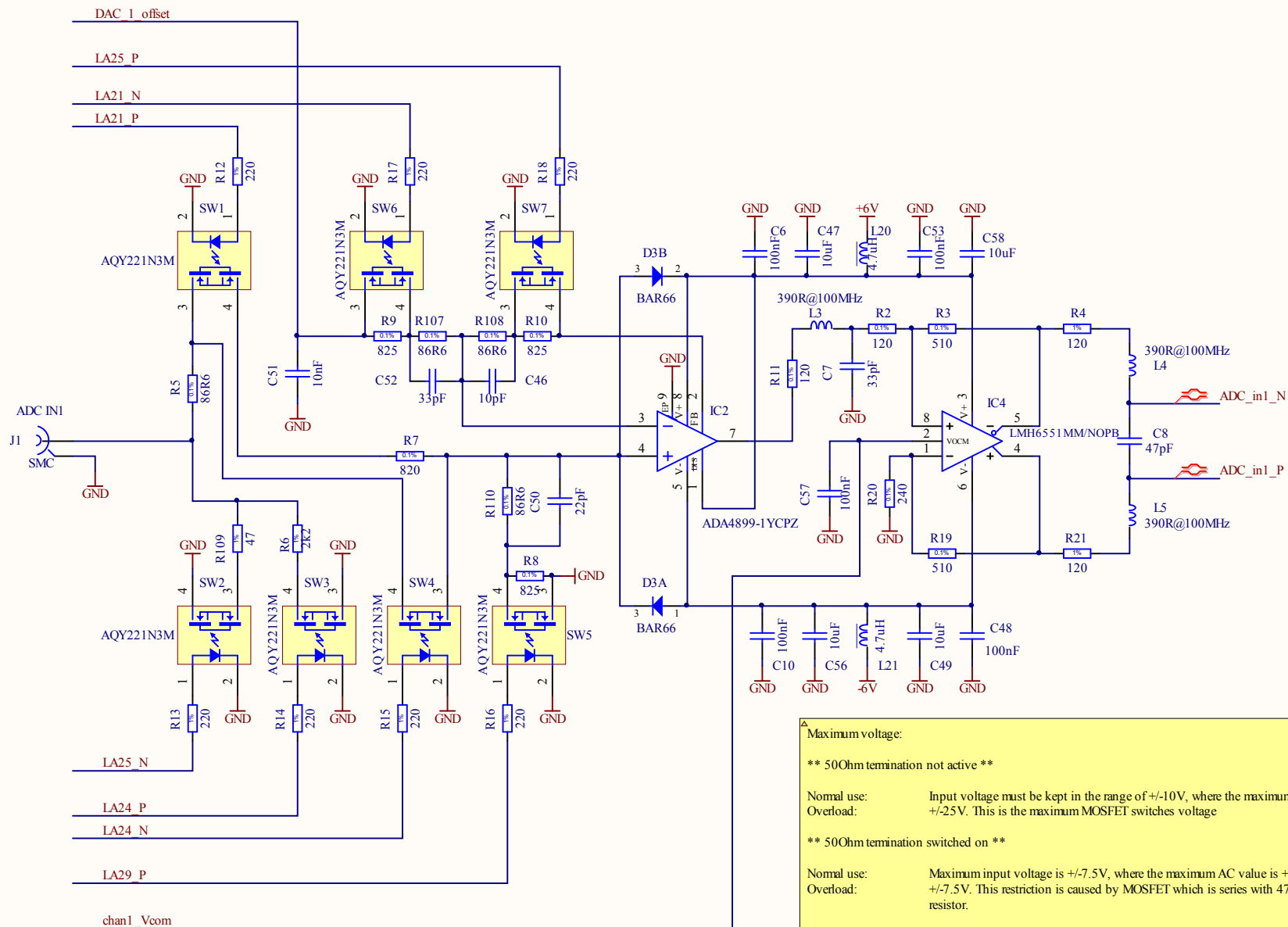




**Maximum voltage:**

**\*\* 500 Ohm termination not active \*\***

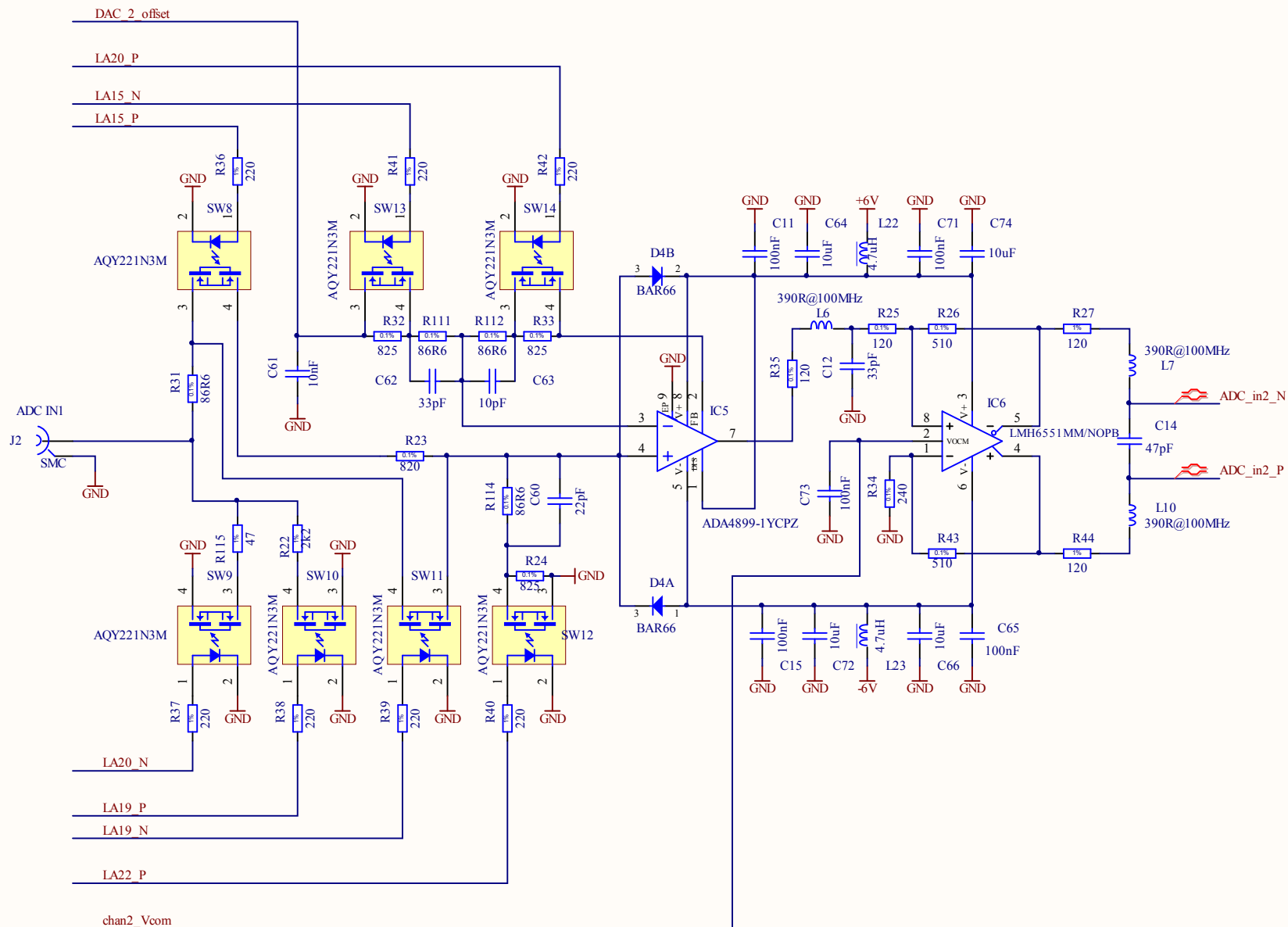
Normal use: Input voltage must be kept in the range of  $\pm 10V$ , where the maximum AC value is  $\pm 5V$ .  
 Overload:  $\pm 25V$ . This is the maximum MOSFET switches voltage

**\*\* 500 Ohm termination switched on \*\***

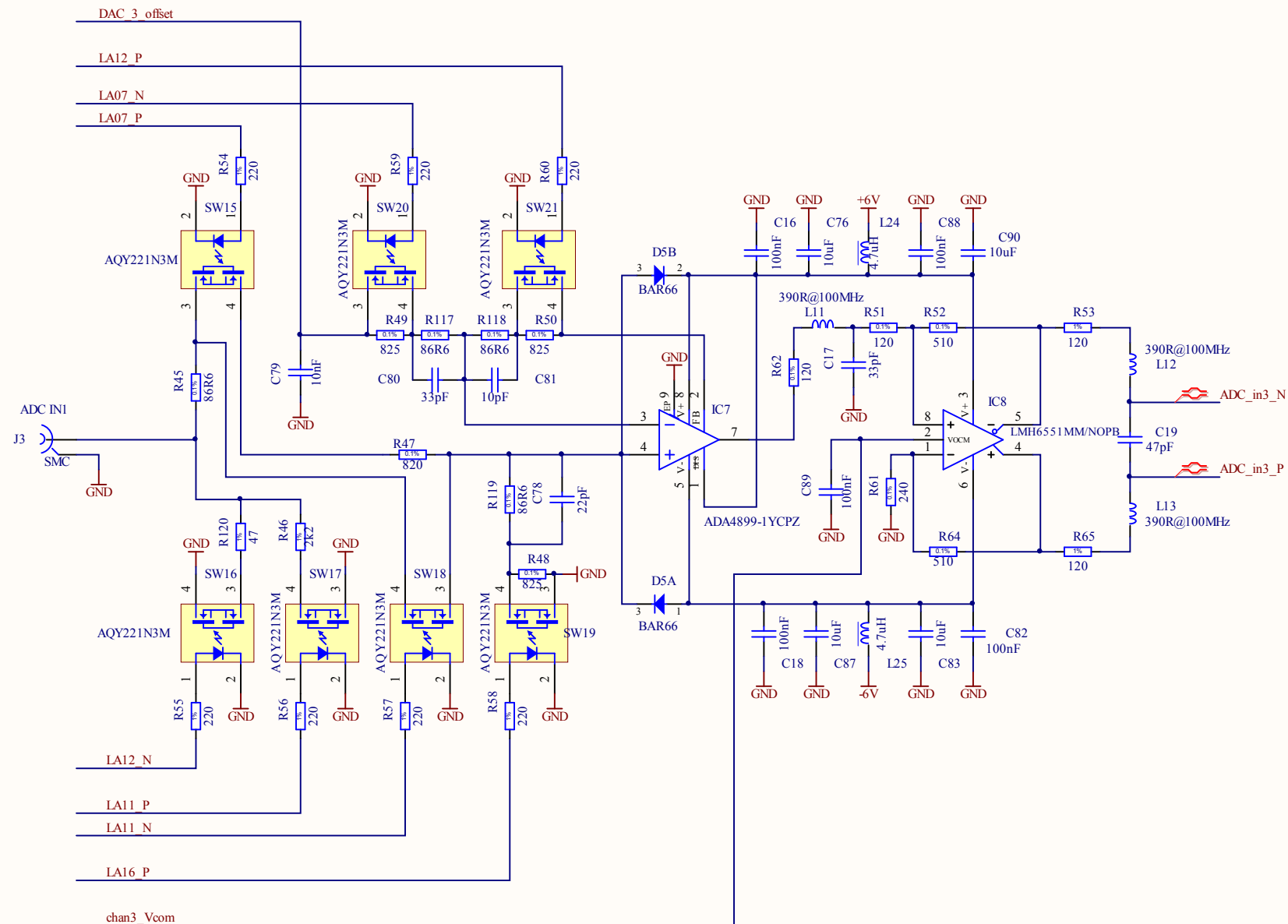
Normal use: Maximum input voltage is  $\pm 7.5V$ , where the maximum AC value is  $\pm 5V$ .  
 Overload:  $\pm 7.5V$ . This restriction is caused by MOSFET which is series with 470 Ohm terminating resistor.

Overload may take only short time. Otherwise it may cause input resistors overheat even if input voltage or current

|                                                                               |                      |                                                                                                                                            |                                                                                    |
|-------------------------------------------------------------------------------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| Project/Equipment                                                             |                      | FmcAdc100M14b4cha                                                                                                                          |                                                                                    |
| Document                                                                      |                      | <div> <div> <div>ENICE</div> <div>CERN</div> </div> <div> <div>Input stage 1</div> <div>Amplifier and trigger receiver</div> </div> </div> |                                                                                    |
| Designer                                                                      | Designer             | 01/02/2010                                                                                                                                 |                                                                                    |
| Drawn by                                                                      | Maciej Fimiars       | -                                                                                                                                          |                                                                                    |
| Check by                                                                      | N.Lopez              | 12.03.2010                                                                                                                                 |                                                                                    |
| Last Mod.                                                                     | -                    |                                                                                                                                            |                                                                                    |
| File                                                                          | input_stage_1.SchDoc |                                                                                                                                            |                                                                                    |
| Print Date                                                                    | 12.03.2010 11:20:34  | Sheet                                                                                                                                      | 01 of 11                                                                           |
| European Organization for Nuclear Research<br>CH-1211 Genève 23 - Switzerland |                      | EDA-02063-V1-0                                                                                                                             | <div> <div>See</div> <div>Rev</div> </div> <div> <div>A4</div> <div>-</div> </div> |

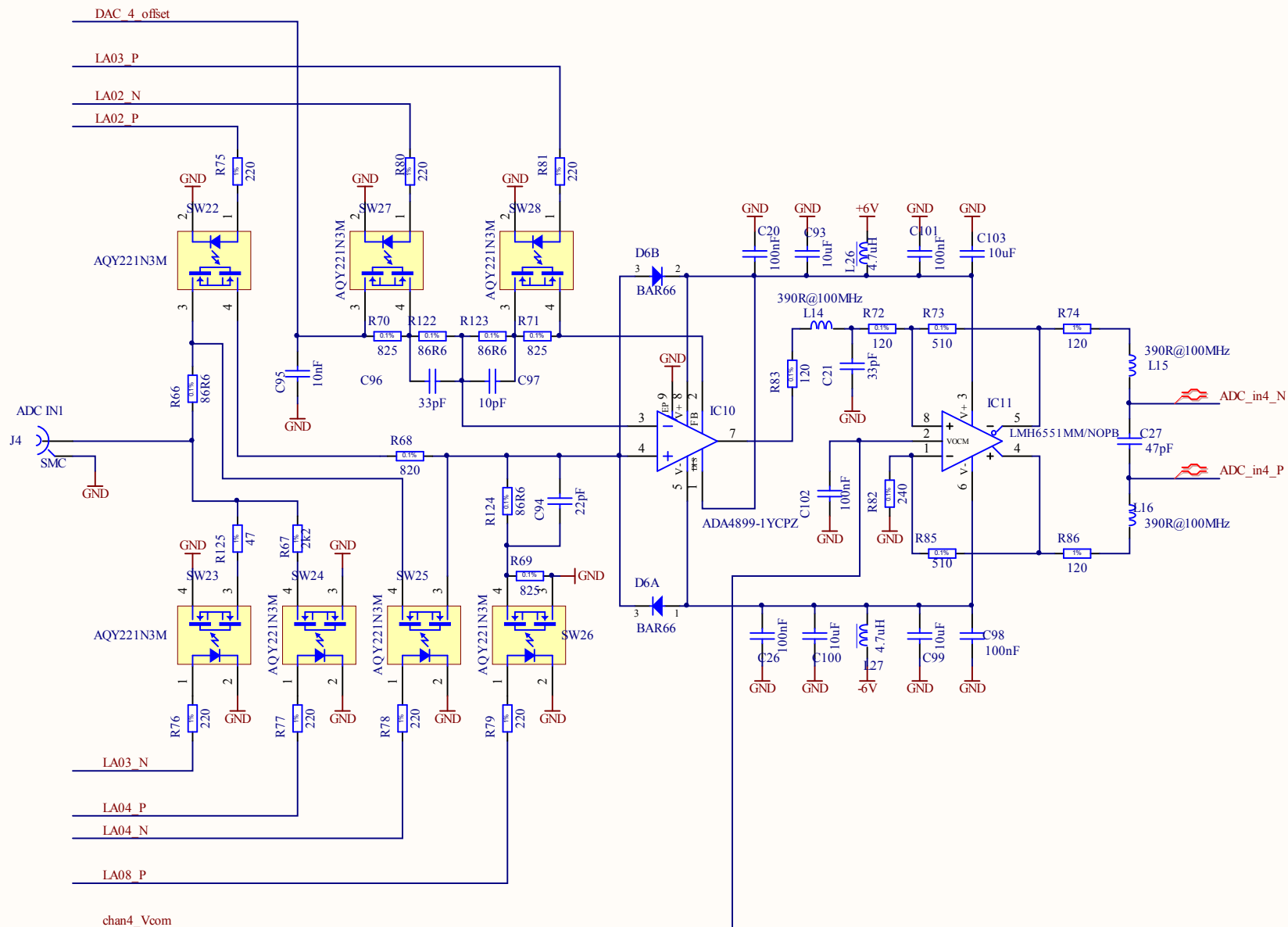


|                          |  |                                                                                                                                                                                                                  |  |
|--------------------------|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| Project/Equipment        |  | FmcAdc100M14b4cha                                                                                                                                                                                                |  |
| Document                 |  | <p>Designer Designer</p> <p>Drawn by Maciej Fimiarz 01/02/2010</p> <p>Check by N.Lopez -</p> <p>Last Mod. - 12.03.2010</p> <p>File input_stage_2.SchDoc</p> <p>Print Date 12.03.2010 11:20:34 Sheet 02 of 11</p> |  |
| <p>ENICE</p> <p>CERN</p> |  | <p><b>Input stage 2</b></p> <p><b>Amplifier and trigger receiver</b></p> <p>European Organization for Nuclear Research</p> <p>CH-1211 Genève 23 - Switzerland</p>                                                |  |
| EDA-02063-V1-0           |  | <p>Size A4</p> <p>Rev -</p>                                                                                                                                                                                      |  |



|                                                                                                                                                                                                                                                     |  |                   |                      |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-------------------|----------------------|
| Project/Equipment                                                                                                                                                                                                                                   |  | FmcAdc100M14b4cha |                      |
| Document                                                                                                                                                                                                                                            |  | Designer Designer |                      |
| <div> <div>ENICE</div> <div>CERN</div> </div> <div> <b>Input stage 3</b><br/> <b>Amplifier and trigger receiver</b> </div> <div>           European Organization for Nuclear Research<br/>           CH-1211 Genève 23 - Switzerland         </div> |  | Drawn by          | Maciej Fimiarz       |
|                                                                                                                                                                                                                                                     |  | Check by          | N.Lopez              |
|                                                                                                                                                                                                                                                     |  | Last Mod.         | -                    |
|                                                                                                                                                                                                                                                     |  | File              | input_stage_3.SchDoc |
|                                                                                                                                                                                                                                                     |  | Print Date        | 12.03.2010 11:20:35  |
|                                                                                                                                                                                                                                                     |  | Sheet             | 03 of 11             |
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EDA-02063-V1-0



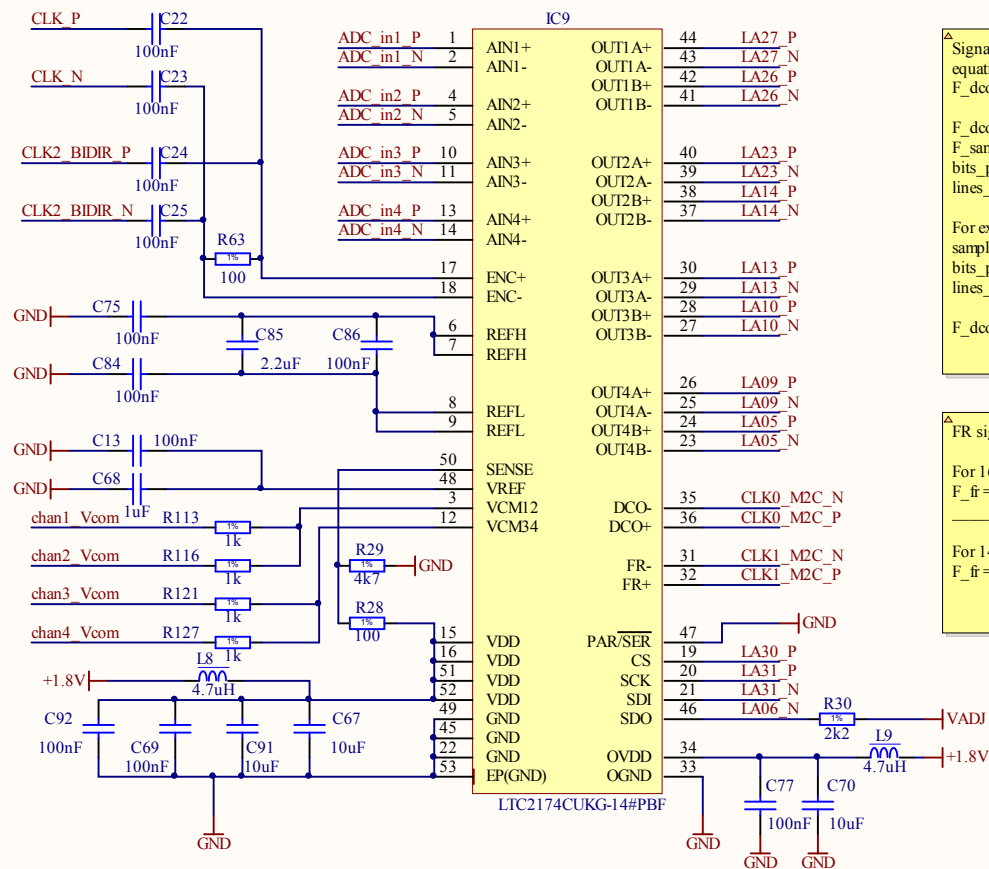
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|-------------------|--|--------------------------------|----------------|
| Project/Equipment |  | FmcAdc100M14b4cha              |                |
| Document          |  | Designer Designer              |                |
| ENICE             |  | Drawn by Maciej Fimiarz        | 01/02/2010     |
| CERN              |  | Check by N.Lopez               | -              |
|                   |  | Last Mod. -                    | 12.03.2010     |
|                   |  | File input_stage 4.SchDoc      |                |
|                   |  | Print Date 12.03.2010 11:20:35 | Sheet 04 of 11 |
|                   |  | Size A4                        | Rev -          |

## **Input stage 4** **Amplifier and trigger receiver**

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EDA-02063-V1-0

For normal use, don't mount C1 and C2.  
For testing purpose remove C3 and C4 and solder C1 and C2. Clock needs to be delivered via not dedicated LA01 pair.



Signal frequency from DCO (CLK0\_M2C) is given by following equation:  
 $F_{dco} = F_{sampling} * bits\_per\_sample / lines\_per\_channel / 2$

F\_dco - frequency of DCO signal  
F\_sampling - ADC sampling frequency  
bits\_per\_sample - 14 (typical) or 16 (compatibility mode)  
lines\_per\_channel - 1 or 2 (typical) pairs for each channel

For example  
sampling freq. - 100MSPs  
bits\_per\_sample - 14  
lines\_per\_channel - 2

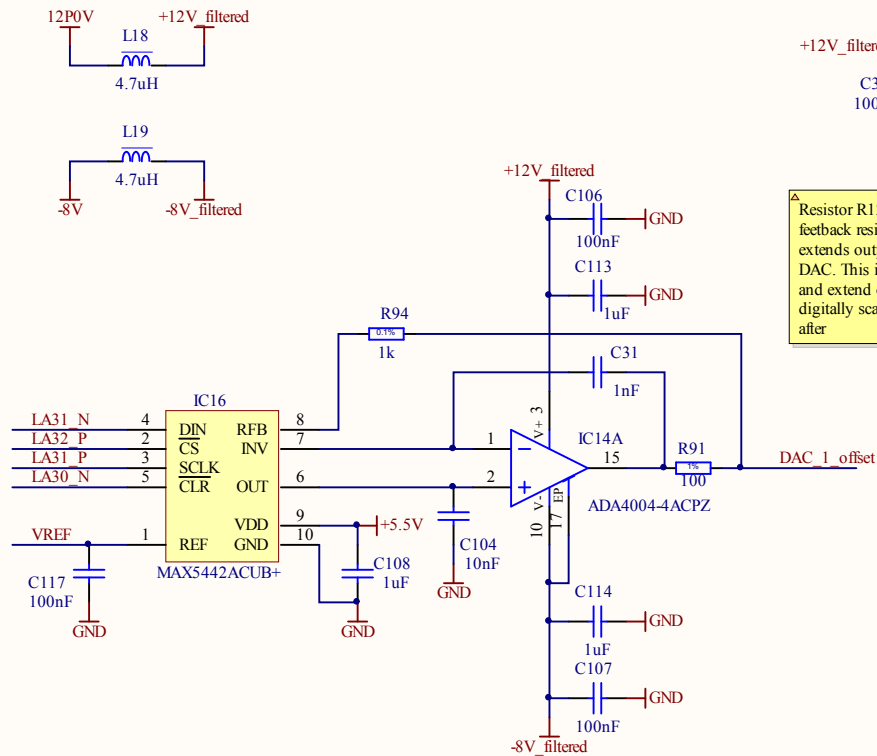
F\_dco = 350MHz

FR signal frequency

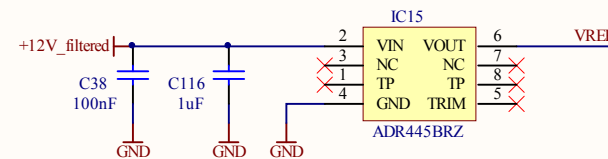
For 16 bit output word length:  
 $F_{fr} = F_{sampling}$

For 14 bit output word length:  
 $F_{fr} = F_{sampling} / 2$

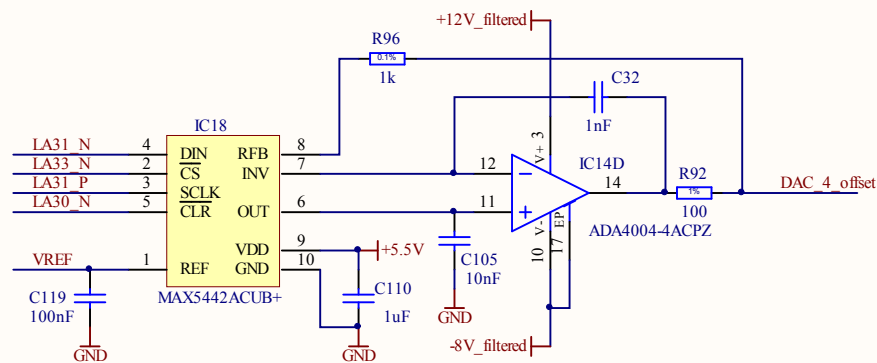
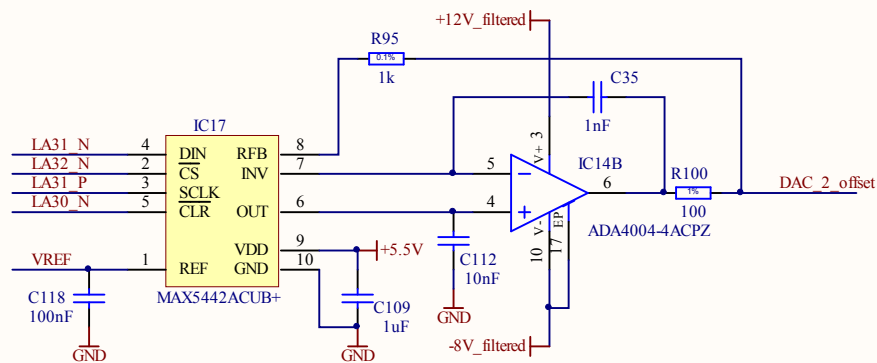
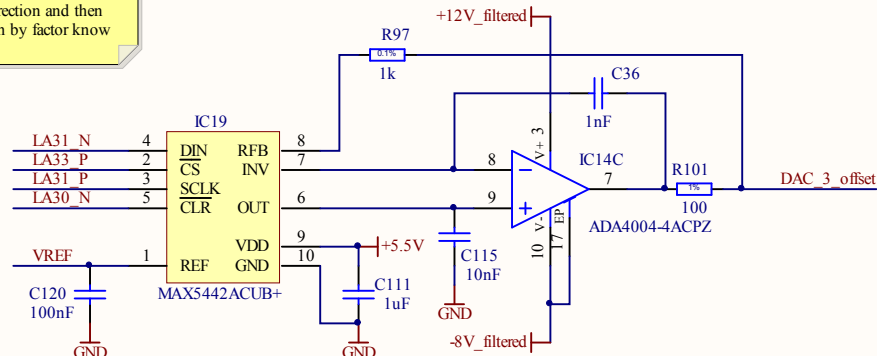
|                                            |  |                                |                |
|--------------------------------------------|--|--------------------------------|----------------|
| Project/Equipment                          |  | FmcAdc100M14b4cha              |                |
| Document                                   |  | Designer Designer              |                |
| ENICE                                      |  | Drawn by Maciej Fimiarz        | 01/02/2010     |
| CERN                                       |  | Check by -                     | -              |
| Linear Technologies' ADC                   |  | Last Mod. -                    | 12.03.2010     |
| 105MSPS 14b                                |  | File ADC.SchDoc                |                |
| European Organization for Nuclear Research |  | Print Date 12.03.2010 11:20:36 | Sheet 05 of 11 |
| CH-1211 Genève 23 - Switzerland            |  | EDA-02063-V1-0                 | See Rev        |
|                                            |  | A4                             | -              |



Resistor R120 added in series with feedback resistors (in the DAC) extends output voltage range of the DAC. This is necessary to achieve and extend offset correction and then digitally scale it down by factor know after



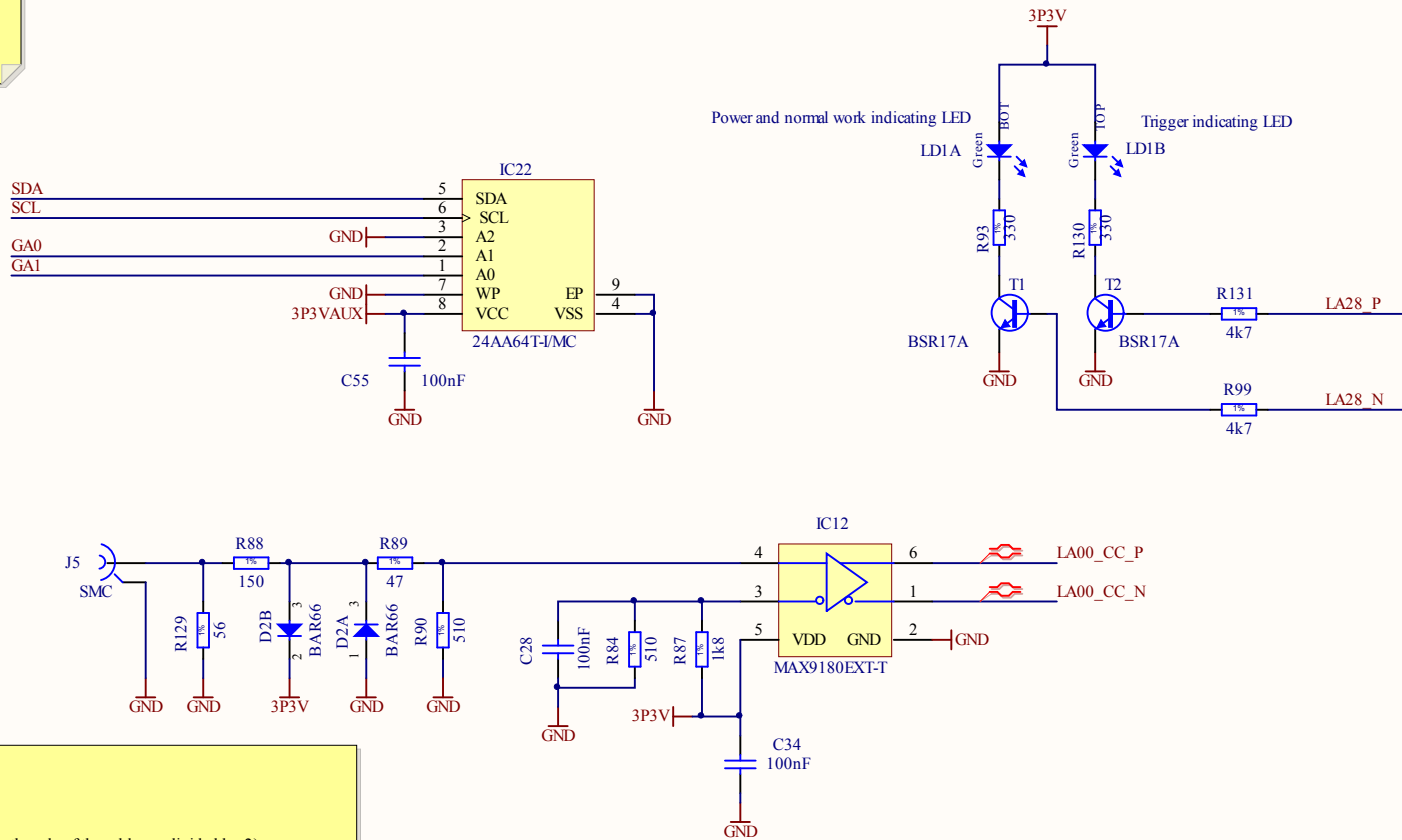
VREF is 5V.



|                                                                               |           |                                               |                |
|-------------------------------------------------------------------------------|-----------|-----------------------------------------------|----------------|
| Project/Equipment                                                             |           | FmcAdc100M14b4cha                             |                |
| Document                                                                      |           | DACs and Vref source<br>for offset correction |                |
|                                                                               | Designer  | Designer                                      | 01/02/2010     |
|                                                                               | Drawn by  | Maciej Fimiarz                                | -              |
|                                                                               | Check by  | -                                             | 12.03.2010     |
|                                                                               | Last Mod. | -                                             | -              |
|                                                                               | File      | DAC.SchDoc                                    | -              |
| Print Date                                                                    |           | 12.03.2010 11:20:36                           | Sheet 06 of 11 |
| European Organization for Nuclear Research<br>CH-1211 Genève 23 - Switzerland |           | EDA-02063-V1-0                                | A4 -           |

24AA64T = 1 0 1 0 0 GA0 GA1  
MCP9801 = 1 0 0 1 0 GA0 GA1

Waming!  
Following the VITA 57.1 standard:  
GA0 goes to A1  
GA1 goes to A0



Threshold voltage:  
- 1V

input voltage range for normal operation:  
min. 1.65V (3.3V with 50Ohm termination on both ends of the cable, so divided by 2)  
max. 5V with termination on both ends of the cable

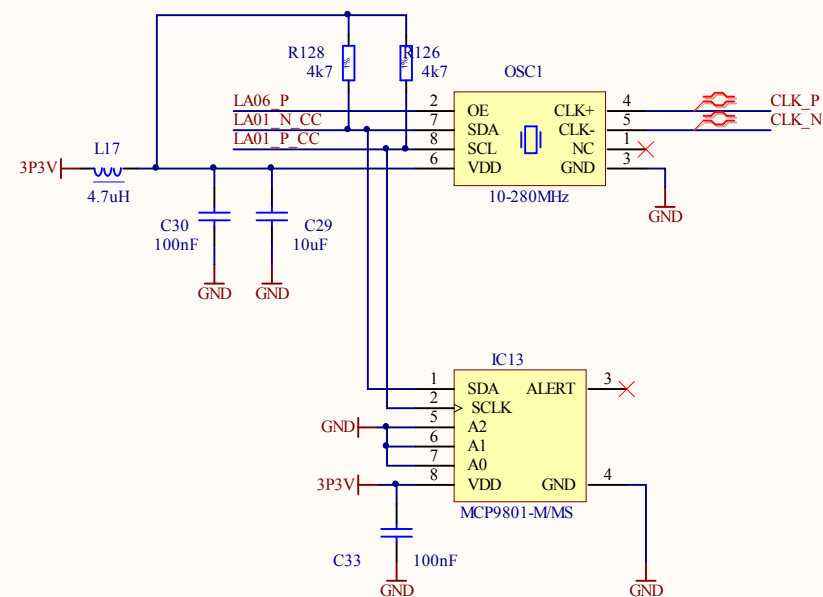
Input is +/- 7.5V tolerant fo continous overload and +/-10V tolerant for short term overload.

|                                                                               |  |                   |                     |
|-------------------------------------------------------------------------------|--|-------------------|---------------------|
| Project/Equipment                                                             |  | FmcAdc100M14b4cha |                     |
| Document                                                                      |  | Designer Designer |                     |
|                                                                               |  | Drawn by          | Maciej Fimiarz      |
|                                                                               |  | Check by          | -                   |
|                                                                               |  | Last Mod.         | -                   |
|                                                                               |  | File              | I2C_mem_LED.SchDoc  |
| European Organization for Nuclear Research<br>CH-1211 Genève 23 - Switzerland |  | Print Date        | 12.03.2010 11:20:36 |
|                                                                               |  | Sheet             | 07 of 11            |
|                                                                               |  | Size              | A4                  |
|                                                                               |  | Rev               | -                   |

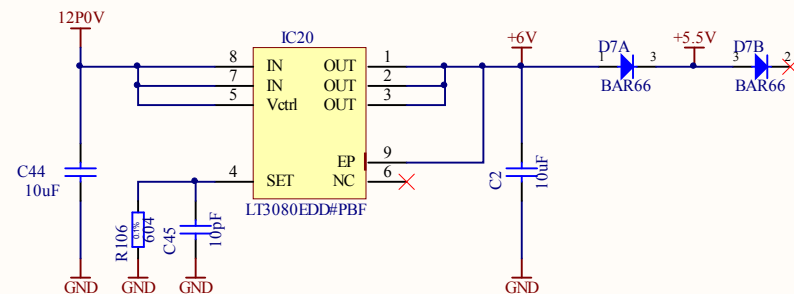
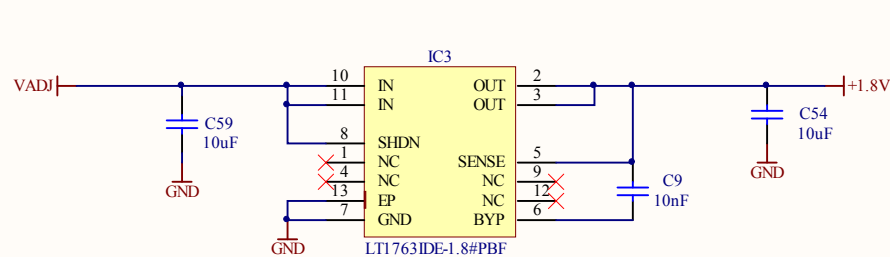
I2C memory and LED indicator

EDA-02063-V1-0

Base address: 0x55    - 1 0 1 0 1 0 1



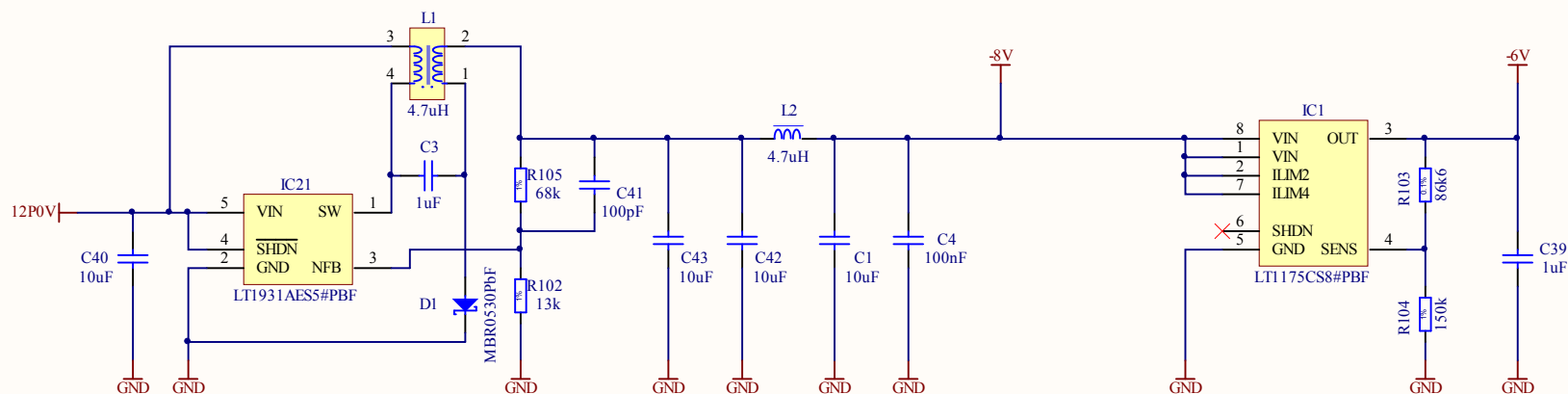
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|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-------------------|------------------------|
| Project/Equipment                                                                                                                                                                                                        |  | FmcAdc100M14b4cha |                        |
| Document                                                                                                                                                                                                                 |  | Designer          | Designer               |
| <br><br><i><b>ADC clock generator</b></i><br>- |  | Drawn by          | Maciej Fimiarz         |
|                                                                                                                                                                                                                          |  | Check by          | -                      |
|                                                                                                                                                                                                                          |  | Last Mod.         | -                      |
|                                                                                                                                                                                                                          |  | File              | clock_generator.SchDoc |
|                                                                                                                                                                                                                          |  | Print Date        | 12.03.2010 11:20:36    |
| European Organization for Nuclear Research<br>CH-1211 Genève 23 - Switzerland                                                                                                                                            |  | Sheet 08 of 11    |                        |
| EDA-02063-V1-0                                                                                                                                                                                                           |  | Size              | A4                     |
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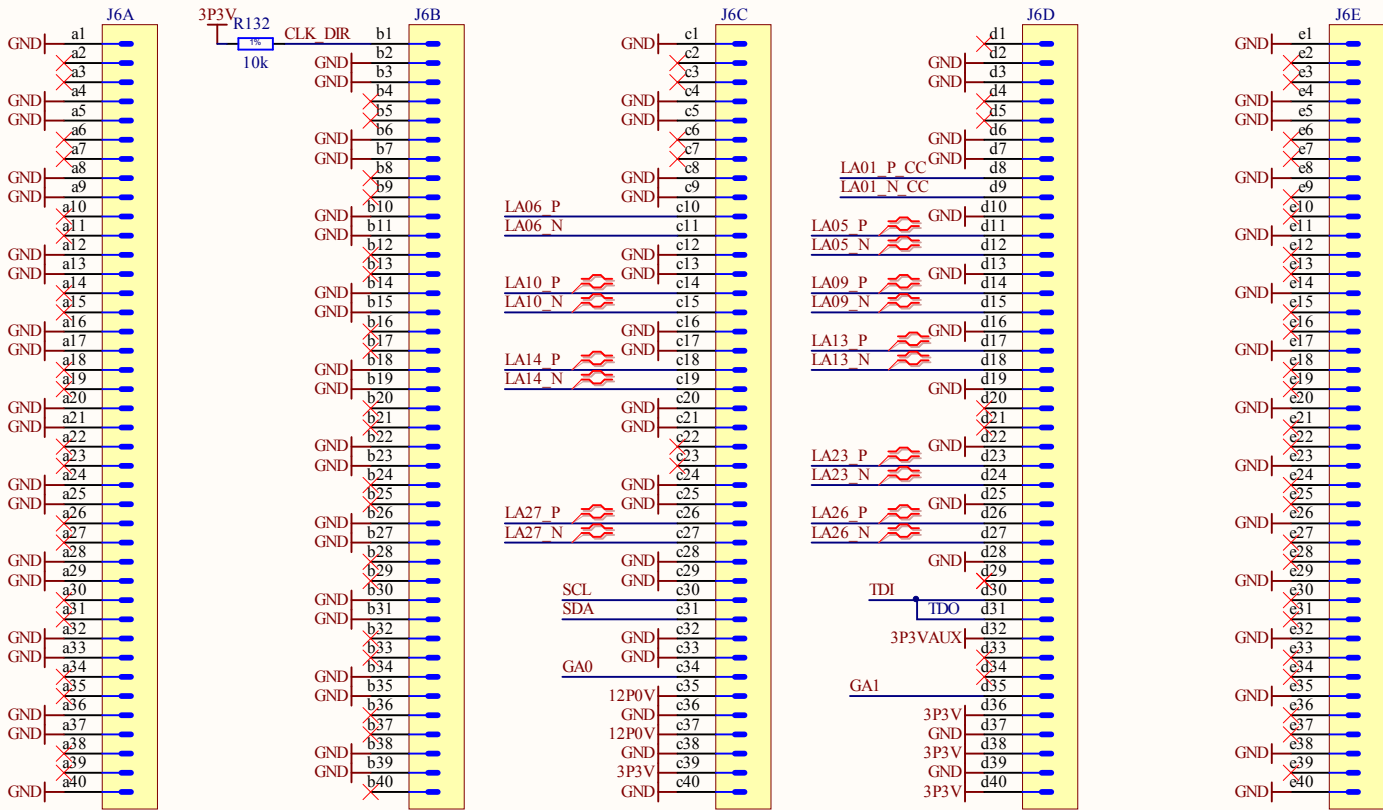
VADJ is set to 2.5V because:

- there is no need of level matching for DAC SPI interface
- FMC board could be tested with Xilinx kit, where VADJ is fixed to 2.5V

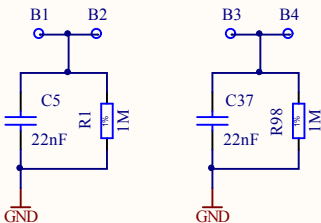
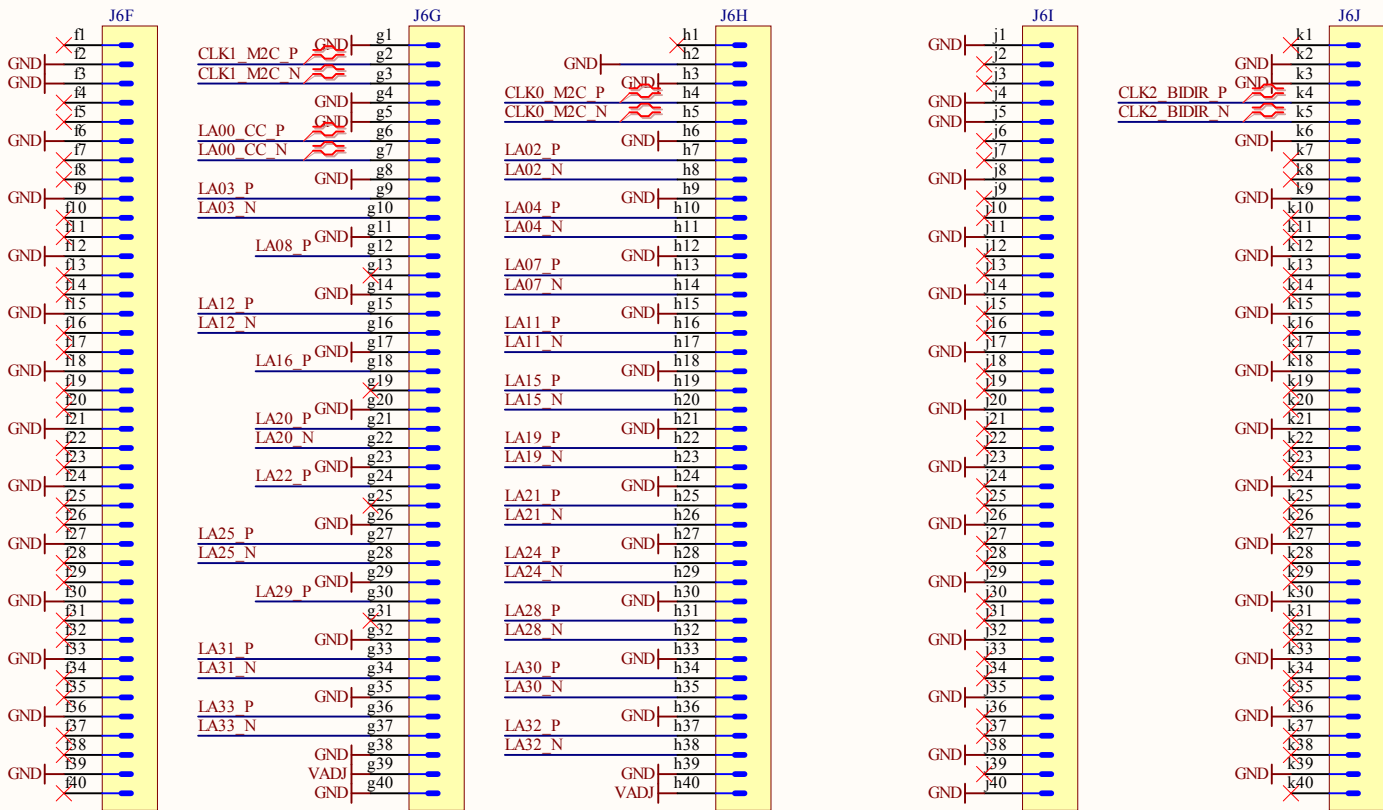
+5.5V is used as a power supply for offset creating DACs. The real value is  $6V - 0.6...0.7V$  which gives 5.3...5.4V. It is lower than 5.5V - max. voltage for normal operation.



|                                                                               |           |                       |                |
|-------------------------------------------------------------------------------|-----------|-----------------------|----------------|
| Project/Equipment                                                             |           | FmcAdc100M14b4cha     |                |
| Document                                                                      |           | <b>Power supplies</b> |                |
|                                                                               | Designer  | Designer              | 01/02/2010     |
|                                                                               | Drawn by  | Maciej Fimiarz        | -              |
|                                                                               | Check by  | -                     | 12.03.2010     |
|                                                                               | Last Mod. | -                     | -              |
|                                                                               | File      | power_supply.SchDoc   | -              |
| Print Date                                                                    |           | 12.03.2010 11:20:37   | Sheet 09 of 11 |
| European Organization for Nuclear Research<br>CH-1211 Genève 23 - Switzerland |           | EDA-02063-V1-0        | See Rev -      |



CC-ended lines are renamed, because Altium Designer treats only P and N ended line names as a differential pairs.



B1 ... B4  
screw holes for mounting the  
FmcAdc to the carrier board.



FTG1 ... FTG6  
Reference points for the  
component mounting machine.

|                   |  |                                            |                         |
|-------------------|--|--------------------------------------------|-------------------------|
| Project/Equipment |  | FmcAdc100M14b4cha                          |                         |
| Document          |  | SAMTEC VITA 57<br>High Pin Count Connector |                         |
| ENICE             |  | Designer                                   | Designer                |
| CERN              |  | Drawn by                                   | Maciej Fimiarz          |
|                   |  | Check by                                   | N.Lopez                 |
|                   |  | Last Mod.                                  | 12.03.2010              |
|                   |  | File                                       | SAMTEC connector.SchDoc |
|                   |  | Print Date                                 | 12.03.2010 11:20:37     |
|                   |  | Sheet                                      | 10 of 11                |
|                   |  | Size                                       | A4                      |
|                   |  | Rev                                        | -                       |

|                              |           |           |           |           |     |     |     |     |
|------------------------------|-----------|-----------|-----------|-----------|-----|-----|-----|-----|
| Switches configuration:      |           |           |           |           |     |     |     |     |
|                              | channel 1 | channel 2 | channel 3 | channel 4 |     |     |     |     |
| sw1                          | LA21_P    | LA15_P    | LA07_P    | LA02_P    |     |     |     |     |
| sw2                          | LA21_N    | LA15_N    | LA07_N    | LA02_N    |     |     |     |     |
| sw3                          | LA25_P    | LA20_P    | LA12_P    | LA03_P    |     |     |     |     |
| sw4                          | LA25_N    | LA20_N    | LA12_N    | LA03_N    |     |     |     |     |
| sw5                          | LA24_P    | LA19_P    | LA11_P    | LA04_P    |     |     |     |     |
| sw6                          | LA24_N    | LA19_N    | LA11_N    | LA04_N    |     |     |     |     |
| sw7                          | LA29_P    | LA22_P    | LA16_P    | LA08_P    |     |     |     |     |
|                              |           | sw1       | sw2       | sw3       | sw4 | sw5 | sw6 | sw7 |
| 100mV range:                 |           | on        | on        | off       | -   | off | on  | off |
| 1V range:                    |           | on        | off       | off       | -   | on  | off | off |
| 10V range:                   |           | on        | off       | on        | -   | off | off | on  |
| DC offset error calibration: |           | off       | off       | off       | off | off | off | on  |
| 50Ohm termination:           |           | -         | -         | -         | on  | -   | -   | -   |

|                                                                            |           |
|----------------------------------------------------------------------------|-----------|
| SPI - SCK                                                                  | LA31_P    |
| SPI - DIN                                                                  | LA31_N    |
| SPI - DAC_RST                                                              | LA30_N    |
| SPI - CS_ADC                                                               | LA30_P    |
| SPI - CS_DAC1                                                              | LA32_P    |
| SPI - CS_DAC2                                                              | LA32_N    |
| SPI - CS_DAC3                                                              | LA33_P    |
| SPI - CS_DAC4                                                              | LA33_N    |
| SPI - SDO_ADC                                                              | LA06_N    |
| LED_TOP                                                                    | LA28_P    |
| LED_BOT                                                                    | LA28_N    |
| Clock generator enable                                                     | LA06_P    |
| Clock generator I2C - SCL                                                  | LA01_P_CC |
| Clock generator I2C - SDA                                                  | LA01_N_CC |
| Lines left unconnected:                                                    |           |
| LA08_N, LA16_N, LA22_N, LA29_N, LA17_P_CC, LA17_N_CC, LA18_P_CC, LA18_N_CC |           |

|                    |              |              |
|--------------------|--------------|--------------|
| Trigger:           | LA00_P_CC    | LA00_N_CC    |
| DCO - output clock | CLK0_M2C_P   | CLK0_M2C_N   |
| FR - frame sync    | CLK1_M2C_P   | CLK1_M2C_N   |
| ADC clock          | CLK2_BIDIR_P | CLK2_BIDIR_N |
| ADC output 1 A     | LA27_P       | LA27_N       |
| ADC output 1 B     | LA26_P       | LA26_N       |
| ADC output 2 A     | LA23_P       | LA23_N       |
| ADC output 2 B     | LA14_P       | LA14_N       |
| ADC output 3 A     | LA13_P       | LA13_N       |
| ADC output 3 B     | LA10_P       | LA10_N       |
| ADC output 4 A     | LA09_P       | LA09_N       |
| ADC output 4 B     | LA05_P       | LA05_N       |

|                                                                                       |  |                   |                          |                |
|---------------------------------------------------------------------------------------|--|-------------------|--------------------------|----------------|
| Project/Equipment                                                                     |  | FmcAdc100M14b4cha |                          |                |
| Document                                                                              |  | Designer Designer |                          |                |
|  |  | Drawn by          | Maciej Fimiarz           | 01/02/2010     |
|                                                                                       |  | Check by          | -                        | -              |
|                                                                                       |  | Last Mod.         | -                        | 08.03.2010     |
|                                                                                       |  | File              | pin_configuration.SchDoc |                |
|                                                                                       |  | Print Date        | 12.03.2010 11:20:37      | Sheet 11 of 11 |
| European Organization for Nuclear Research<br>CH-1211 Genève 23 - Switzerland         |  | EDA-02063-V1-0    |                          | Size A4 Rev -  |