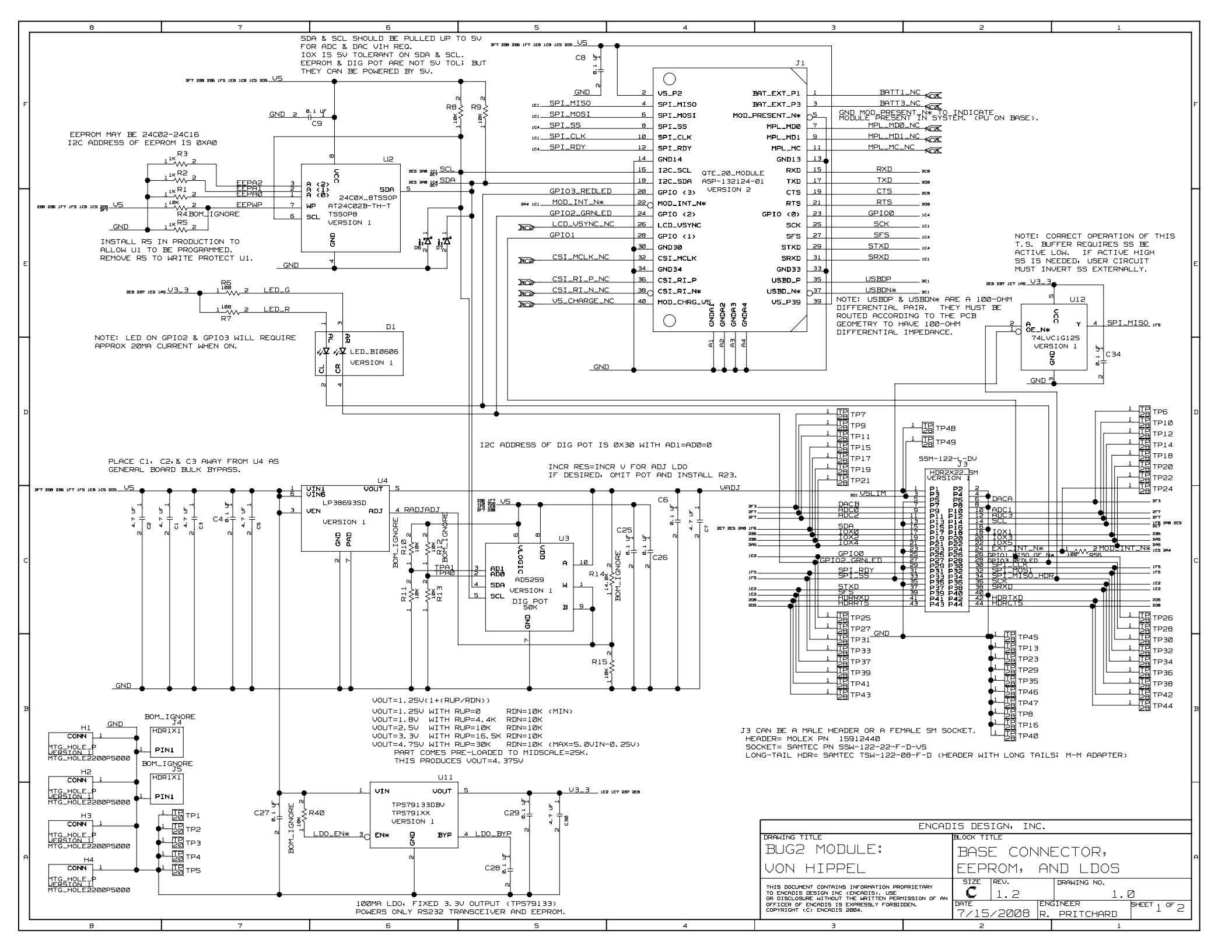
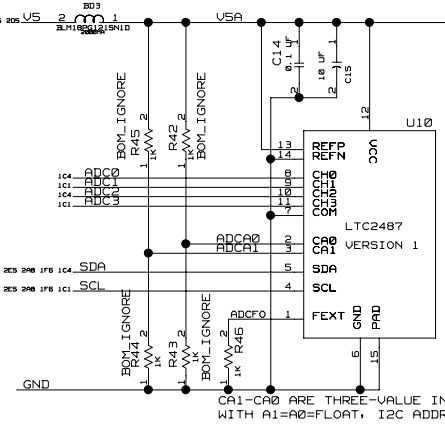
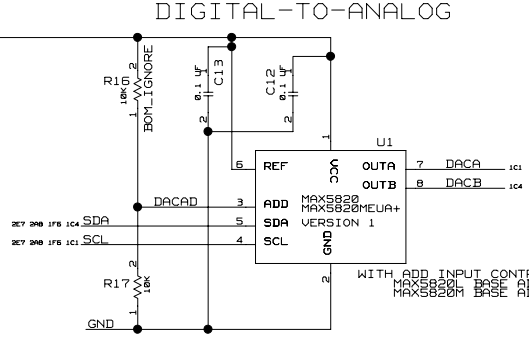

SDA & SCL SHOULD BE PULLED UP TO 5V FOR ADC & DAC VIH REQ.
IOX IS 5V TOLERANT ON SDA & SCL.
EEPROM & DIG POT ARE NOT 5V TOL; BUT THEY CAN BE POWERED BY 5V.
EEPROM MAY BE 24C02-24C16
I2C ADDRESS OF EEPROM IS 0XA0
INSTALL R5 IN PRODUCTION TO ALLOW U1 TO BE PROGRAMMED.
REMOVE R5 TO WRITE PROTECT U1.
NOTE: LED ON GPIO2 & GPIO3 WILL REQUIRE APPROX 20MA CURRENT WHEN ON.
GND MOD_PRESENT_N* TO INDICATE MODULE PRESENT IN SYSTEM. (PU ON BASE).
NOTE: USBDP & USBDN* ARE A 100-OHM DIFFERENTIAL PAIR. THEY MUST BE ROUTED ACCORDING TO THE PCB GEOMETRY TO HAVE 100-OHM DIFFERENTIAL IMPEDANCE.
NOTE: CORRECT OPERATION OF THIS T.S. BUFFER REQUIRES SS BE ACTIVE LOW. IF ACTIVE HIGH SS IS NEEDED, USER CIRCUIT MUST INVERT SS EXTERNALLY.
I2C ADDRESS OF DIG POT IS 0X30 WITH AD1=AD0=0
INCR RES=INCR V FOR ADJ LDO
IF DESIRED, OMIT POT AND INSTALL R23.
PLACE C1, C2, & C3 AWAY FROM U4 AS GENERAL BOARD BULK BYPASS.
VOUT=1.25V(1+(RUP/RDN))
VOUT=1.25V WITH RUP=0 RDN=10K (MIN)
VOUT=1.8V WITH RUP=4.4K RDN=10K
VOUT=2.5V WITH RUP=10K RDN=10K
VOUT=3.3V WITH RUP=16.5K RDN=10K
VOUT=4.75V WITH RUP=30K RDN=10K (MAX=5.0VIN-0.25V)
PART COMES PRE-LOADED TO MIDSCALE=25K.
THIS PRODUCES VOUT=4.375V
J3 CAN BE A MALE HEADER OR A FEMALE SM SOCKET.
HEADER= MOLEX PN 15912440
SOCKET= SAMTEC PN SSW-122-22-F-D-VS
LONG-TAIL HDR= SAMTEC TSW-122-08-F-D (HEADER WITH LONG TAILS; M-M ADAPTER)
100MA LDO, FIXED 3.3V OUTPUT (TPS79133)
POWERS ONLY RS232 TRANSCEIVER AND EEPROM.
J1
QTE_20_MODULE
ASP-132124-01
VERSION 2
U2
24C0X_8TSSOP
AT24C02B-TH-T
TSSOP8
VERSION 1
U3
AD5259
VERSION 1
DIG POT
50K
U4
LP38693SD
VERSION 1
U11
TPS79133DBV
TPS791XX
VERSION 1
U12
74LVC1G125
VERSION 1
D1
LED_BI0606
VERSION 1
J3
SSM-122-L-DV
HDR2X22_SM
VERSION 1
J4
J5
ENCADIS DESIGN, INC.
DRAWING TITLE
BUG2 MODULE:
VON HIPPEL
BLOCK TITLE
BASE CONNECTOR,
EEPROM, AND LDOS
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COPYRIGHT (C) ENCADIS 2004.
SIZE C
REV. 1.2
DRAWING NO. 1.0
DATE 7/15/2008
ENGINEER R. PRITCHARD
SHEET 1 OF 2

ANALOG-TO-DIGITAL



CA1-CA0 ARE THREE-VALUE INPUTS, H, L, FL.
WITH A1=A0=FLOAT, I2C ADDR IS 0X48

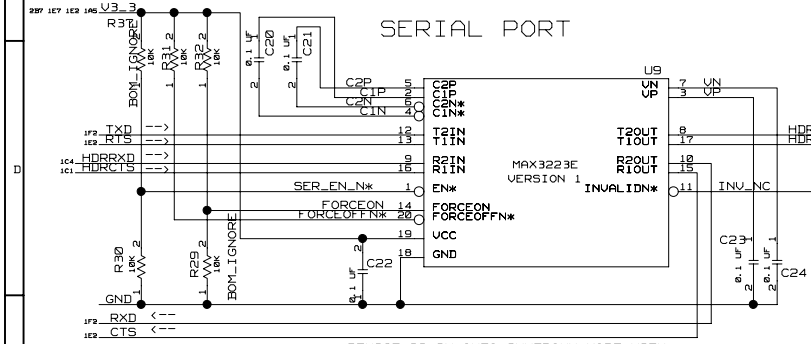
DIGITAL-TO-ANALOG



WITH ADD INPUT CONTROL: 0 1
MAX5820L BASE ADDR: 0X70 0X71
MAX5820M BASE ADDR: 0XB0 0XB1

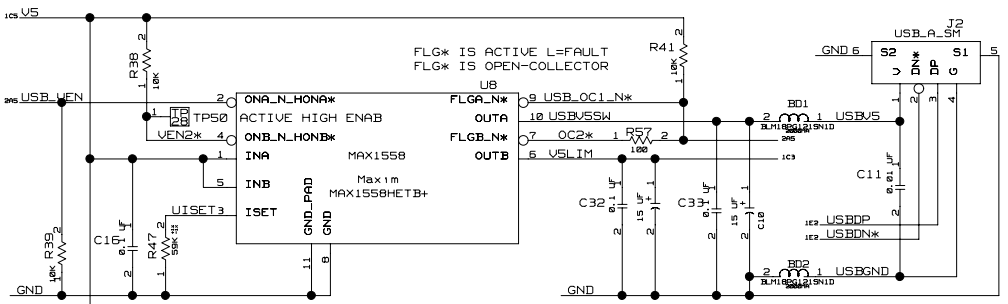
WE'RE USING M WITH ADD=0, SO I2C ADDR=0XB0

SERIAL PORT



DEVICE IS IN AUTO-SHUTDOWN MODE WITH
FORCEON=L AND FORCEOFF*=H.
SET FORCEON=H TO DISABLE AUTO-SHUTDOWN.
AUTO-SHUTDOWN IS VERY LOW ISUPPLY WHEN INACTIVE.

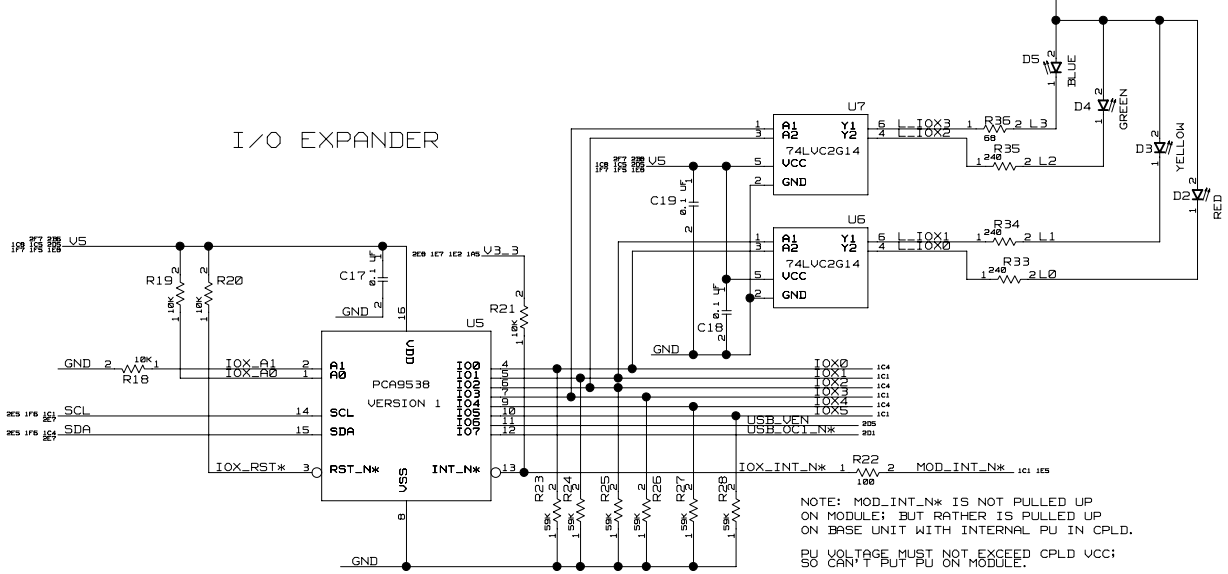
USB CONNECTOR & POWER CONTROL



FLG* IS ACTIVE L=FAULT
FLG* IS OPEN-COLLECTOR

NOTE: USBDP AND USBDN* ARE A DIFFERENTIAL
PAIR, CONTROLLED IMPEDANCE 100 OHMS.

I/O EXPANDER



2G14 VOL = 0.55V

		FOR 20MA:	FOR 10MA:
BLU: 3.6V	VRES = 0.85V	R = 42.5	R = 85
GRN: 2.2V	VRES = 2.25V	R = 112.5	R = 225
YEL: 2.0V	VRES = 2.45V	R = 122.5	R = 245
RED: 2.0V	VRES = 2.45V	R = 122.5	R = 245

NOTE: MOD_INT_N* IS NOT PULLED UP
ON MODULE; BUT RATHER IS PULLED UP
ON BASE UNIT WITH INTERNAL PU IN CPLD.

PU VOLTAGE MUST NOT EXCEED CPLD VCC;
SO CAN'T PUT PU ON MODULE.

IOX_INT AND INT FROM HDR ARE WIRE-OR'ED
ON MODULE & SENT TO BASE UNIT.

I2C I/O EXPANDER DEVICE ADDR=0XE2

ENCADIS DESIGN, INC.

DRAWING TITLE: BUG2 MODULE: VON HIPPEL	BLOCK TITLE: IOX + LEDS; DAC; ADC; SERIAL PORT; USB CONN.
SIZE: C	REV.: 1.2
DRAWING NO.: 1.0	
DATE: 7/15/2008	ENGINEER: R. PRITCHARD
SHEET 2 OF 2	

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