
ML8953A

Preliminary

3-axis Accelerometer

ML8953A

**Datasheet for the 3-axis Accelerometer
with Digital Output**

TABLE OF CONTENTS

1.	GENERAL DESCRIPTION	4
2.	ELECTRIC CHARACTERISTICS	5
2.1	Maximum ratings	5
2.2	Recommended operating conditions	6
2.3	Current consumption	7
2.4	Digital DC characteristics	7
2.5	Input/Output capacitances	7
2.6	Internal oscillator characteristic	8
2.7	AC characteristics	8
2.7.1	System reset	8
2.7.2	Interrupt	9
2.7.3	SPI interface	10
2.7.4	I ² C interface	12
2.7.5	Accessing register in SPI and I ² C modes	13
2.8	Power-on and off	14
3.	Functional description	15
3.1	Table of pin descriptions	15
3.2	Circuit constructions	16
3.3	Package dimensions	17
3.4	Output directions in the accelerometer	17
3.5	Example of host interfacing (M-8953 - Host)	18
3.6	SPI interface	20
3.7	I ² C bus interface	22
4.	REGISTERS	23
4.1	List of registers	23
4.1.1	Table of page 0 registers (For setup)	23
4.1.2	Table of page 1 registers (Result registers)	24
4.1.3	Table of Page 6 registers (General purpose registers)	24
4.2	Register descriptions	25
4.2.1	Explanation of bits in registers	25
4.2.2	Table of page 0 registers	26
4.2.3	Table of page 1 registers	27
4.2.4	Table of page 6 registers	28
4.3	Details of registers	29
4.3.1	Page 0 registers	29
4.3.1.1	Device reset register (PAGE0 / 01h): DVRST	29
4.3.1.2	Power-down register for oscillator (PAGE0 / 02h): PDWN	29
4.3.1.3	Operation mode control register 0 (PAGE0 / 03h): CTRL0	30

4.3.1.4	Sensor measurement mode register 0 (PAGE0 / 05h): MODE0.....	32
4.3.1.5	Sensor measurement mode register 1 (PAGE0 / 06h): MODE1.....	35
4.3.1.6	Sensor interrupt request register (PAGE0 / 07h): INTREQ	36
4.3.1.7	Sensor interrupt mask setting register (PAGE0 / 08h): INTMSK.....	41
4.3.1.8	Timer data register for automatic measurement mode (PAGE0 / 09~0Ah): TMD	43
4.3.1.9	Configuration register (PAGE0 / 0Ch): CFG	44
4.3.1.10	g detection interrupt output condition settings (PAGE0 / 0Dh): INTOTM.....	45
4.3.1.11	Data averaging in automatic acceleration measurement mode (PAGE0 / 0Eh): GAAVE.....	47
4.3.1.12	Data averaging in normal acceleration measurement mode (PAGE0 / 0Fh): GNAVE	48
4.3.1.13	g detection threshold level setting register (PAGE0 / 11~14h): GDTCT0/1.....	49
4.3.1.14	CPU ready register (PAGE0 / 15h): CPURDY.....	50
4.3.1.15	Register page selection register (1Eh): PGSEL	50
4.3.2	Page 1 register.....	51
4.3.2.1	Status register (PAGE1 / 01h): STATUS	51
4.3.2.2	g vector register for automatic measurement mode (PAGE1 / 02~07h): GAX/Y/Z.....	51
4.3.2.3	Acceleration composite vector register for automatic measurement mode (PAGE1 / 08~09h): GASV 52	
4.3.2.4	g vector register for normal measurement mode (PAGE1 / 0A~0Fh): GNX/Y/Z	52
4.3.2.5	Acceleration composite vector register for normal measurement mode (PAGE1 / 10~11h): GNSV 53	
4.3.2.6	Tilt angle result register (PAGE1 / 12~15h): PITCH, ROLL	54
4.3.2.7	Temperature calculation result storage register (PAGE1 / 19~1Ah): TEMP.....	56
4.3.3	Page 6 registers.....	57
4.3.3.1	General purpose registers 0 (PAGE6 / 01~09h)	57
4.3.3.2	General purpose registers 1 (PAGE6 / 0A~11h)	57
5	GENERAL CONTROL FLOW	58
5.1	Initialization.....	58
5.2	Temperature measurement.....	59
5.3	Measuring acceleration (No pitch/roll angle calculation).....	60
5.4	Measuring acceleration (Including pitch/roll angle calculation)	61
5.5	Automatic measurement	62
5.6	Offset adjustment.....	64
5.6.1	Performing offset adjustment.....	64
5.6.2	Loading of reference offset and sensitivity in re-powering up	68
6	ELECTRIC CHARACTERISTICS.....	70
6.1	Current consumption diagram in acceleration measurement (Including calculation).....	70
6.2	Diagram of current consumption in calculation.....	70
6.3	Diagram of current consumption in automatic measurement during interval between measurements.....	71
7	AUTOMATIC ACCELERATION MEASUREMENT MODE AND INTERRUPT MEASUREMENT.....	72

1. GENERAL DESCRIPTION

The ML8953A is a 3-axis accelerometer based on the piezo-resistive sensing principle and that provides data output in a digital format.

The ML8953A features internal automatic pitch and roll calculation by the built-in LSI, thus taking the burden off the host controller to perform the trigonometric calculations. The ML8953A with its internal signal control LSI offers the users ease-to-use functionality reducing software developing resources.

The ML8953A is fabricated using advanced MEMS (Microelectromechanical Systems) technology achieving microminiaturization and low cost products.

FEATURES

- The built-in LSI calculates pitch and roll internally, thus eliminating the need to perform angle calculation by the host controller.
- Built-in automatic dynamic and static acceleration measuring function
- Composite and tri-axis acceleration are calculated by the built-in LSI including temperature compensation capability.
- Piezoresistive tri-axis accelerometer
- Ceramic package (Ceramic QFN 5.0×5.0×1.15mm)
- Low voltage drive (Digital section supply voltage: 1.8 V to V_{DDA} , Analog section supply voltage: 2.5 to 3.6 V)
- Digital outputs to interface with host controller (SPI, I²C)
- Several Operational Modes: Continuous (with average function), g detection, interrupt mode, composite output

APPLICATIONS

- Menu navigation (scrolling) for user interface in handheld devices
- Automatic power turn on/off function (Input switch)
- Posture control for robots or other machines
- Game controllers, motion sensors
- Pedometer
- Abnormal vibration detection
- Fall/drop detection
- Security

MAIN SPECIFICATIONS

- Acceleration measurement range: ± 3 g
- Output accuracy: ± 0.1 g (at 1g)
- Pitch and Roll: $\pm 180.0^\circ$
- Digital output interfaces: Serial communication output (SPI: 7 MHz @Max. speed, I²C: 400 kHz)
- Response frequency: 200Hz
- Sensitivity: 100~170 LSB/g
- Linearity: 5% of full scale
- Operating current: 200 ~ 300 μ A (Typical in Polled Operation Mode@30 msec interval time)
- Standby current: 1 μ A (Typical)

Note:

If in case output shift is beyond tolerance your application targets, it is recommended to readjust the offset externally. Please refer for the readjustment procedures to section 5.6.

ORDERING PART NUMBER

Package: 18-pin ceramic QFN (ML8953A-04AFC)

2. ELECTRIC CHARACTERISTICS

2.1 Maximum ratings

Parameter	Symbol	Condition		Rating	Unit	Pin name
Maximum Acceleration	GMAX	Any axis, 0.1ms		5000	g	-
Supply voltage (analog)	VDDA	Ta = +25°C		-0.3 ~ +6.0	V	avdd
Supply voltage (Digital I/O)	VDDD	agnd = 0V		-0.3 ~ +6.0	V	dvdd
Digital input voltage	VDIN	exthv = 0V		-0.3 ~ VDDD+0.3	V	See note
Analog input voltage	VAIN			-0.3 ~ VDDA+0.3	V	See note
Digital input current	IDI		dvdd = 3.0V	-10 ~ +10	mA	See note
Digital output current	IDO			-10 ~ +10	mA	See note
Allowable loss	PD	Ta = +25°C		1000	mW	-
Storage temperature	TSTG	-		-30 ~ +125	°C	-

Note:

- Analog power pin and digital power pin are represented as avdd and dvdd, respectively.
- Refer to pins with a letter of D in the table pin descriptions if parameters for digital.
- Refer to pins with a letter of A in the table of pin descriptions if parameters for analog.

 Stress above those listed as “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 Recommended operating conditions

agnd = dgnd = 0V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin name
Supply voltage (Analog)	V_{DDA}		2.5	3.0	3.6	V	avdd
Supply voltage (Digital I/O)	V_{DDD}		1.78	3.0	V_{DDA}	V	dvdd
Operating temperature (Accelerometer)	T_{aa}	-	-20	+25	+70	°C	
SPI digital input rise time	t_{IRIS}		-	-	5	ns	Digital input pin
SPI digital input fall time	t_{IFIS}		-	-	5	ns	Digital input pin
I ² C digital input rise time	t_{IRIS}		-	-	300	ns	Digital input pin
I ² C digital input fall time	t_{IFIS}		-	-	300	ns	Digital input pin
Digital output load	C_{DL}		-	-	50	pF	Digital input pin
SPI clock input frequency	F_{SCLK}	i2c_mode=0	0		7	MHz	sclk_sclk
SPI clock input duty rate	D_{SCLK}	i2c_mode=0	45	50	55	%	sclk_scl
I ² C clock input frequency	F_{SCL}	i2c_mode=1	0		400	kHz	sclk_scl
I ² C clock input L period	L_{SCL}	i2c_mode=1	1.3	-	-	μs	sclk_scl
I ² C clock input H period	H_{SCL}	i2c_mode=1	0.6	-	-	μs	sclk_scl

Note:

- Please also refer to the sections for DC and AC characteristics for recommended operating conditions.
- For digital input pins, refer to the pins with a letter of DI in the table of pin descriptions.
- For digital output pins, refer to the pins with a letter of DO in the table of pin descriptions.
- About supply voltages, please use the following conditions. The operating conditions and electric characteristics are determined within the given range. If supply voltages are beyond these limits, the electric characteristics may not be guaranteed, or the sensors may not operate properly.

$V_{DDA} = 2.5V \sim 3.6V$, $V_{DDD} = 1.78 \sim 3.6$, $V_{DDD} \leq V_{DDA}$, dgnd = agnd = 0V

2.3 Current consumption

$V_{DD}=1.78 \sim 3.6V$, $V_{DDA}=2.5 \sim 3.6V$, and $= dgnd = 0V$, $T_a = -20$ to $70^{\circ}C$

Parameter	Symbol	Min.	Typ.	Max.	Unit	Pin name
In power down	I_{DDs}	-	1	20	μA	-
Measurement start process and including or excluding pitch and roll calculation (See figure in section 6.2)	I_{DD1}	-	10	30	mA	-
Automatic measurement mode interval	I_{DD2}	-	150	250	μA	-
In measuring accelerometer	I_{DD3}	-	2.5	4.5	mA	-

Note:

- Current consumption in power down refers to the condition when the internal oscillator stops by setting power down register after disabling reset.

2.4 Digital DC characteristics

$V_{DD}=1.78 \sim 3.6V$, $V_{DDA}=2.5 \sim 3.6V$, $agnd = dgnd = 0V$, $T_a = -20$ to $70^{\circ}C$

Parameter	Symbol	Measuring condition	Min.	Max.	Unit	Pin name
High level input voltage	V_{IH}		$V_{DD} \times 0.8$	$V_{DD} + 0.3$	V	DI/DIO
Low level input voltage	V_{IL}		-0.3	$V_{DD} \times 0.25$	V	DI/DIO
Hysteresis width	V_{HS1}	$V_{DD} \leq 2V$	$V_{DD} \times 0.05$	-	mV	DI/DIO
	V_{HS2}	$V_{DD} > 2V$	$V_{DD} \times 0.1$	-	mV	DI/DIO
High level output voltage	V_{OH}	$I_{OH} = -3mA$	$V_{DD} - 0.4$	V_{DD}	V	DO/DIO
Low level output voltage	V_{OL1}	$I_{OL} = 3mA$	0	0.36	V	DO/DIO
Input leakage current 1	I_L	$V_{IL} = 0$, $V_{IH} = V_{DD}$	-5	+5	μA	All pins
Input leakage current 2	I_{PU}	$V_{IL} = 0$	-130	-2	μA	resetn

2.5 Input/Output capacitances

$V_{DD}=1.78 \sim 3.6V$, $V_{DDA}=2.5 \sim 3.6V$, $agnd = dgnd = 0V$, $T_a = -25$ to $70^{\circ}C$, $f=1MHz$

Parameter	Symbol	Measuring condition	Min.	Max.	Unit	Pin name
Input capacitance at digital input pin	C_{IN}		-	20	pF	DI/DIO
Output capacitance at digital output pin	C_{OUT}		-	20	pF	DO/DIO

2.6 Internal oscillator characteristic

$V_{DD}=1.78 \sim 3.6V$, $V_{DDA}=2.5 \sim 3.6V$, $agnd = dgnd = 0V$, $T_a = -25 \text{ to } 70^{\circ}C$

Parameter	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Frequency	FOSC	-	5.45	6.2	6.94	MHz

2.7 AC characteristics

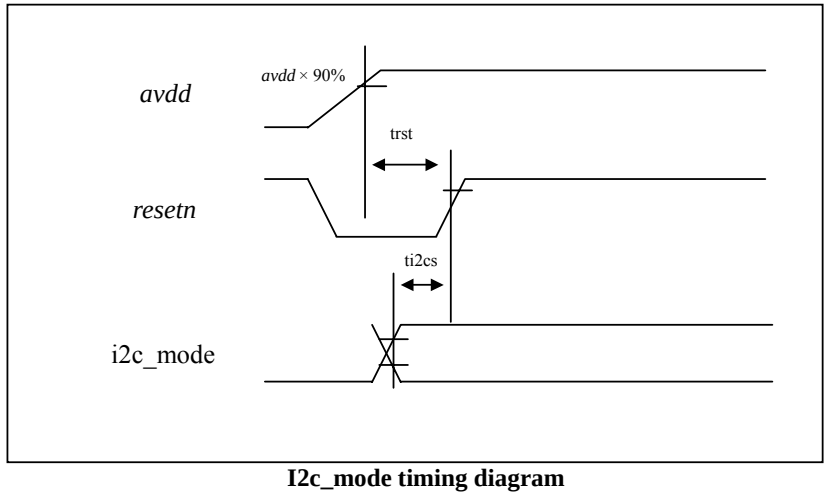
2.7.1 System reset

$V_{DD}=1.78 \sim 3.6V$, $V_{DDA}=2.5 \sim 3.6V$, $agnd = dgnd = 0V$, $T_a = -20 \text{ to } 70^{\circ}C$

Parameter	Symbol	Measuring condition	Min.	Max.	Unit	Pin name
Reset time	trst	After reaching $90\% \times avdd$	1	-	ms	resetn
Serial mode setup time	ti2cs	-	250	-	ns	i2c_mode
Serial interface access allowable time after disabling reset	tind	After disabling the reset and reaching $90\% \times avdd$		2.1	ms	
Analog power down time after disabling reset	tina	After disabling the reset and reaching $90\% \times avdd$		10	μs	

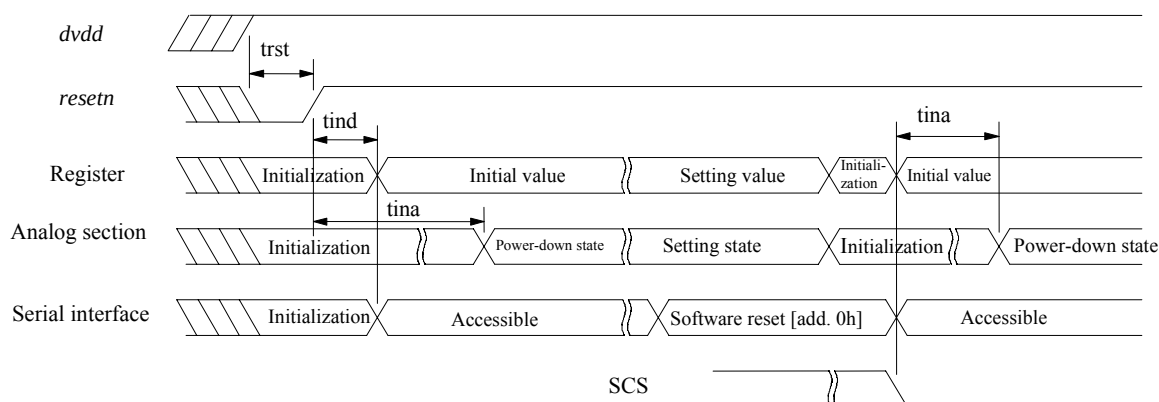
Note:

- Timing in measurement is determined at voltage levels of $V_{DD} \times 20\%$, $V_{DD} \times 80\%$, except *trst* for *avdd* is not the case.
- Reset with the *resetn* pin must be performed upon power-up. Operation is not guaranteed if reset is not carried out.

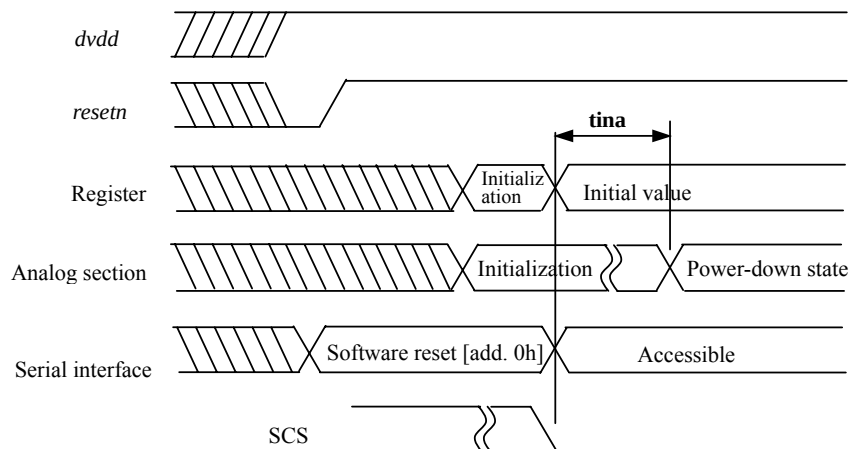


Note:

- If *i2c_mode* signal is changed after reset is finished, the operation is not guaranteed.
- Reset with the *resetn* pin must be performed upon power-up. Operation is not guaranteed if reset is not carried out.
- It is necessary for the reset to keep low signal level until analog power, digital power and regulator voltage become stable.



Reset timing diagram



Software reset timing diagram

The ML8953A has two types of reset, hardware reset and software reset activated by writing into the internal register. Hardware reset must be performed to guarantee correct operation of the device.

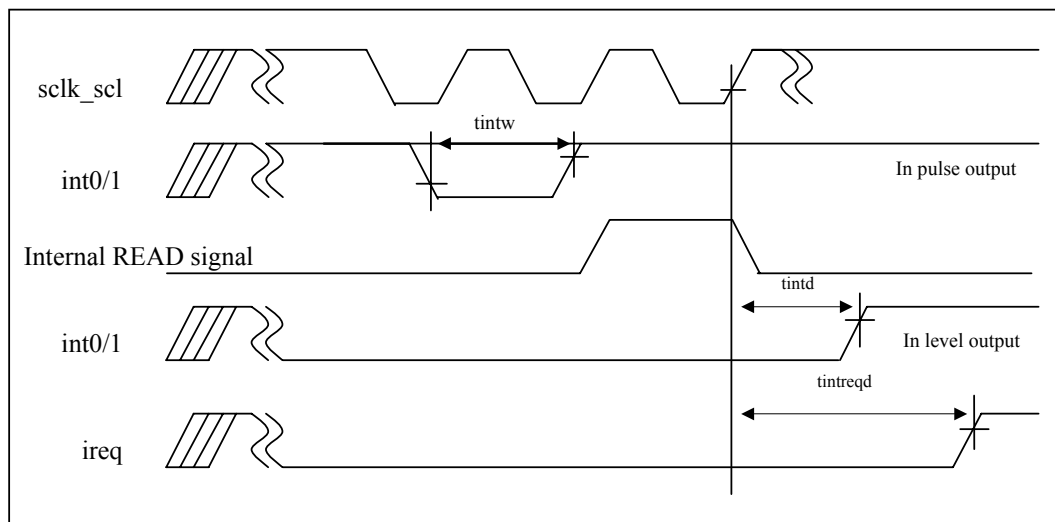
2.7.2 Interrupt

$V_{DD} = 1.78 \sim 3.6V$, $V_{DDA} = 2.5 \sim 3.6V$, $agnd = dgnd = 0V$, $T_a = -20$ to $70^\circ C$

Parameter	Symbol	Measuring condition	Min.	Max.	Unit	Pin name
INT0/1 LOW period (Pulse output selected)	tintw	-	100	-	ns	int0/1
INT0/1 clear delay time (Level output selected)	tintd	$C_{load} = 50pF$	-	$t_{sk} \times 2 + 30$	ns	int0/1
INT_REQ internal register Clear delay time	tintreqd	-	-	2	μs	-

Note:

- Timing is determined at voltage levels of $V_{DD} \times 20\%$, $V_{DD} \times 80\%$.



Interruption clearing timing diagram

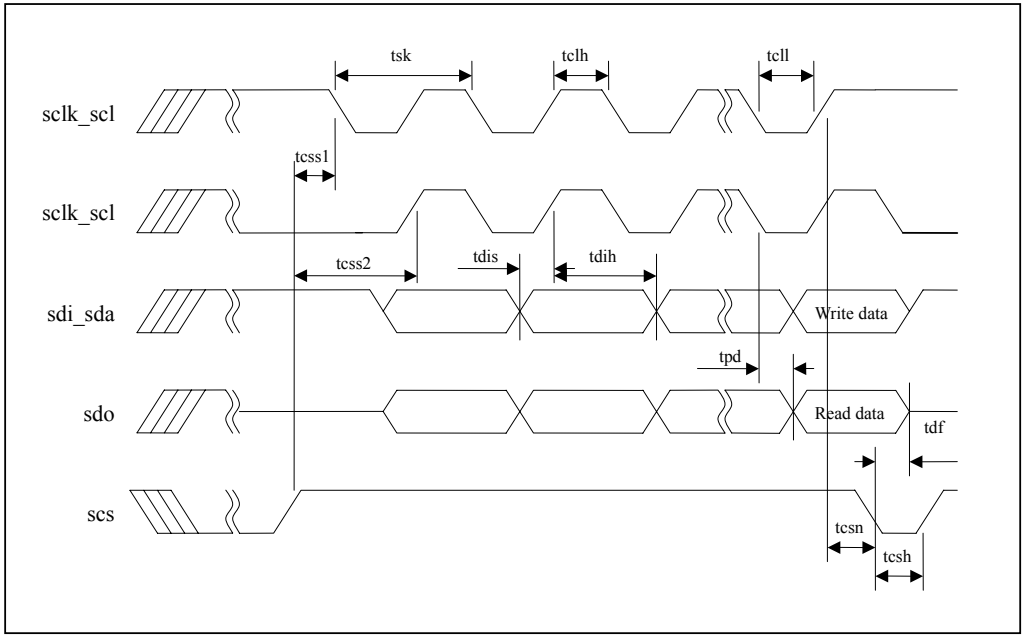
2.7.3 SPI interface

$V_{DD} = 1.78 \sim 3.6V$, $V_{DDA} = 2.5 \sim 3.6V$, $agnd = dgnd = 0V$, $T_a = -20$ to $70^\circ C$

Parameter	Symbol	Measuring condition		Min.	Max.	Unit	Pin name
sclk cycle time (Default)	tsk	V _{DD} ≥2.0V		142	-	ns	sclk_scl
		V _{DD} <2.0V		200	-	ns	
sclk duty cycle	DCLK	-		45	55	%	sclk_scl
scs low period	tclsh	-		142	-	ns	scs
scs setup time	tcss1	-		13+tsk/2	-	ns	scs
scs setup time	tcss2	-		13+tsk		ns	scs
scs hold time	tcsn	-		13+tsk		ns	scs
sdi_sda setup time	tdis	-		13		ns	sdi_sda
sdi_sda hold time	tdih	-		13		ns	sdi_sda
sdo delay time	tpd	C _{load} =50pf	V _{DD} ≥2.0V	-	58	ns	sdo
			V _{DD} <2.0V	-	80	ns	
sdo delay time	tdf	C _{load} =50pf	V _{DD} ≥2.0V	-	58	ns	sdo
			V _{DD} <2.0V	-	80	ns	

Note:

- Timing is determined at voltage levels of $V_{DD} \times 20\%$, $V_{DD} \times 80\%$.
- The values in the table are valid when sdo (4-wire mode) or sdi_sda (3-wire mode) is set to H/L output mode. When the open-drain mode is set, the value in output delay becomes larger due to an external circuit connected. In order to ensure data acquisition, it may be necessary to reduce the SPI clock frequency.



SPI timing diagram

2.7.5 Accessing register in SPI and I²C modes

In SPI and I²C modes, there is difference of operation as a consequence of address area being accessed. The tables below are descriptions how internal operation is carried out when specific address area is accessed in the increment mode set with the CFG register.

- SPI mode

Input address (8 bits)	Operation	After address increment	Operation
00H – 1FH	Writing to 00H – 1FH	00H – 1FH (W)	Writing to 00H – 1FH
20H – 7FH	Access is ignored (High impedance output)	20H – 7FH (W)	Repetitive writing to 00H – 1FH
80H – 9FH	Reading from 00H – 1FH	80H – 9FH I	Reading from 00H – 1FH
A0H – FFH	Access is ignored (High impedance output)	A0H – FF(R)	Repetitive reading from 00H – 1FH

- I²C mode

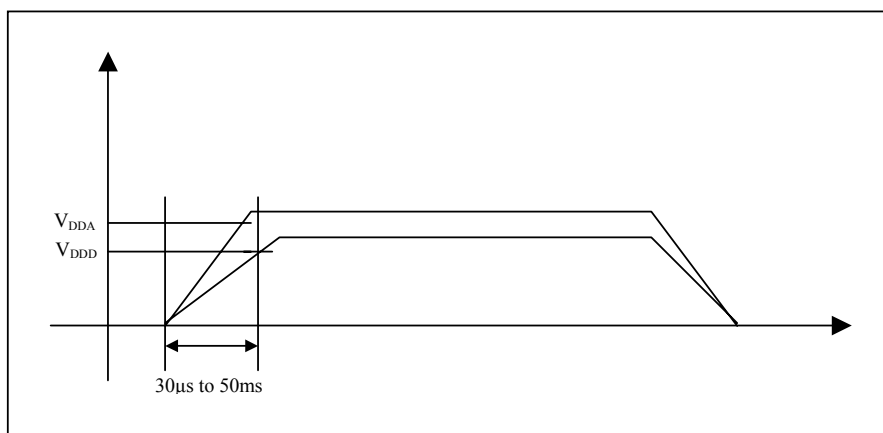
Input address (8 bits)	Operation	After address increment	Operation
00H – 1FH	Accessing to 00H – 1FH	00H – 1FH (W)	Accessing to 00H – 1FH
20H – 7FH	Access is prohibited.	20H – 7FH (W)	Repetitive accessing to 00H – 1FH

2.8 Power-on and off

It is recommended that the power for analog and digital sections be applied simultaneously. If a time delay in power between analog and digital sections can not be avoided, power should be applied to the analog section first. It is also recommended to turn on all power within an interval of 30 μ s and 50 ms.

On power up, reset by the *resetsn* must be performed. Proper operation cannot be guaranteed without this reset.

On power down, it is recommended to turn off all power simultaneously.



Timing diagram of power-on and off

3. Functional description

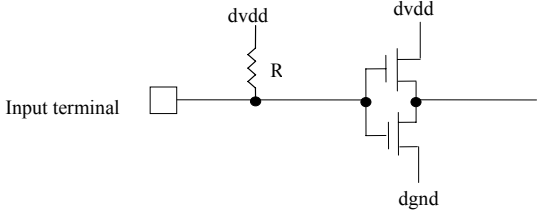
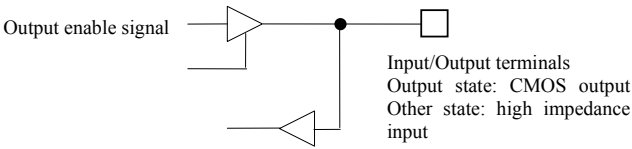
3.1 Table of pin descriptions

Pin No.	Pin name	Input/Output	Function
1	avdd	S	Analog supply voltage (Internal logic voltage only)
2	dvdd	S	Digital supply voltage
3	dgnd	S	Digital ground
4	sclk_scl	DI	SPI : SCLK, I ² C : SCL
5	scs	DI	SPI : SCS (chip select), I ² C : Slave address 0
6	sdi_sda	DIO	SPI : SDI (Input), 3-wire : SDIO (Input/Output) I ² C : SDA (Input/Output)
7	sdo	DIO	SPI : SDO (Output), I ² C : Slave address 1 (Input)
8	i2c_mode	DI	0 : SPI, 1 : I ² C
9	int0	DO	0 : Enable interrupt, 1 : Disable interrupt
10	int1	DO	0 : Enable interrupt, 1 : Disable interrupt
11	test0	-	Connected to analog ground
12	pass	AO	VREF pin
13	test1	-	Connected to digital ground
14	regout	AO	Regulator output pin
15	resetsn	DI	0: Reset
16	NC	-	Internally not connected
17	test2	-	Open
18	agnd	S	Analog ground

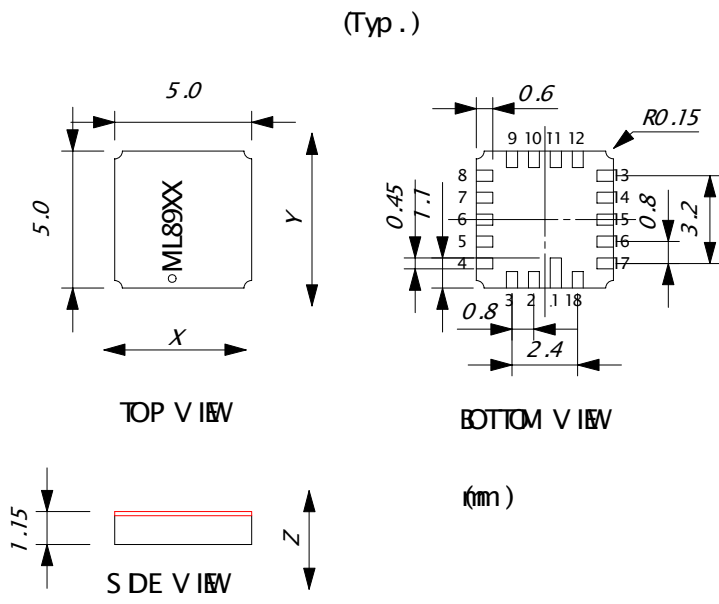
(Symbols)

S: Power supply, DI: Digital input, DO: Digital output, DIO: Digital input/output, AO: Analog output

3.2 Circuit constructions

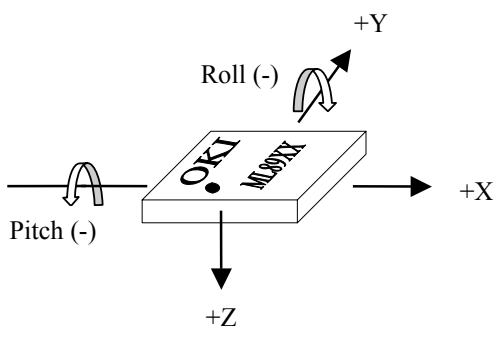
Terminal type	Pin name	Circuit at terminal
Digital input	resetn	
Input/Output terminal	Digital terminals	 <p>Input/Output terminals Output state: CMOS output Other state: high impedance input</p> <p>Note: Open drain NMOS mode is selectable.</p>

3.3 Package dimensions



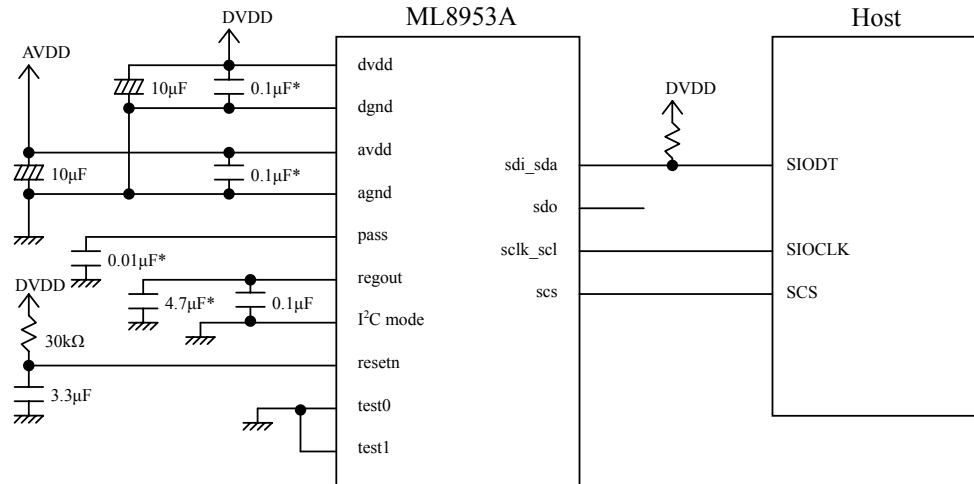
3.4 Output directions in the accelerometer

The arrow indicating a positive direction shows that the corresponding output will increase when acceleration is applied. Pitch and roll are rotational angles around x axis and y axis, respectively.



3.5 Example of host interfacing (M-8953 - Host)

- SPI mode, 3-wire serial connection



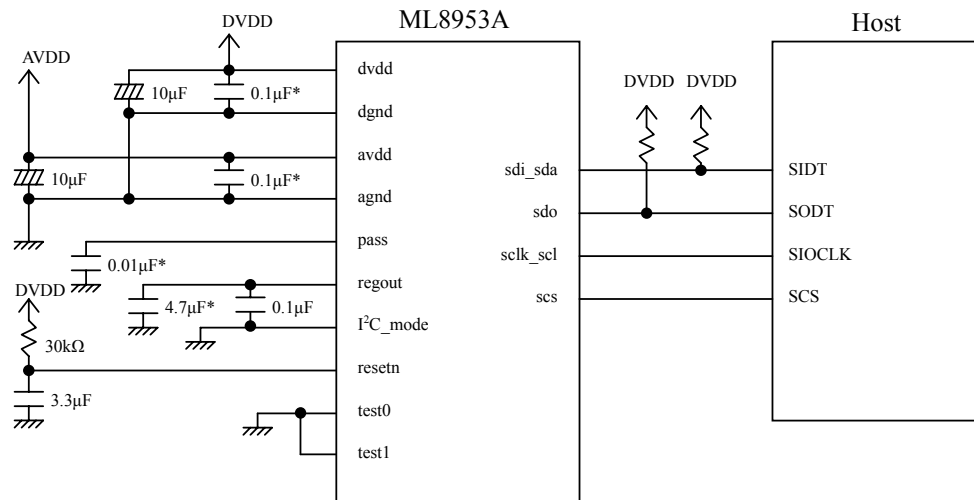
Note:

An external capacitor is required between AVDD and AGND.

Use of 10μF ($\leq \pm 20\%$) and 4.7μF ($\leq \pm 20\%$) aluminum electrolytic or tantalum capacitors (Recommended rated voltage: $\geq 16V$), or 0.1μF ($\leq \pm 20\%$) ceramic capacitors is recommended.

Capacitors indicated with * must be soldered on PCB.

- SPI mode, 4-wire serial connection



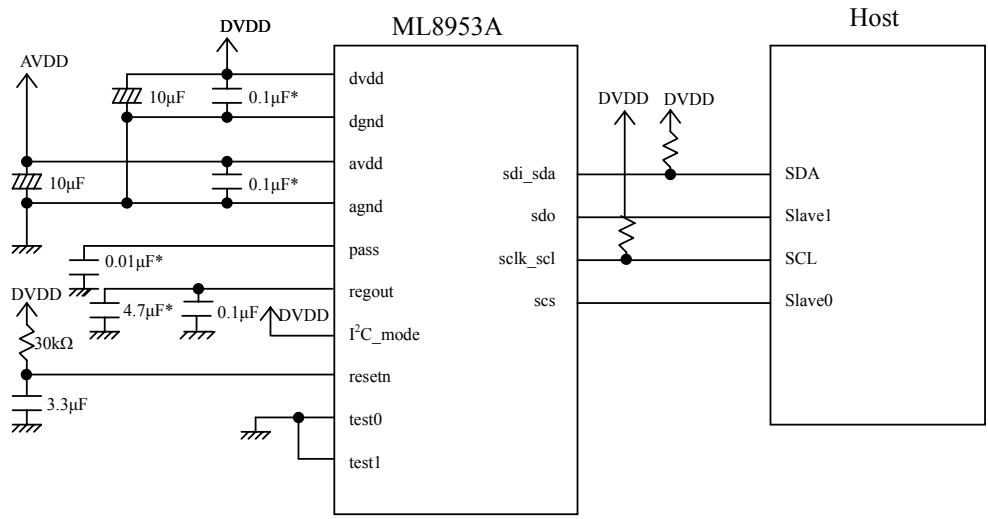
Note:

An external capacitor is required between AVDD and AGND.

Use of 10μF ($\leq \pm 20\%$) and 4.7μF ($\leq \pm 20\%$) aluminum electrolytic or tantalum capacitors (Recommended rated voltage: $\geq 16V$), or 0.1μF ($\leq \pm 20\%$) ceramic capacitors is recommended.

Capacitors indicated with * must be soldered on PCB

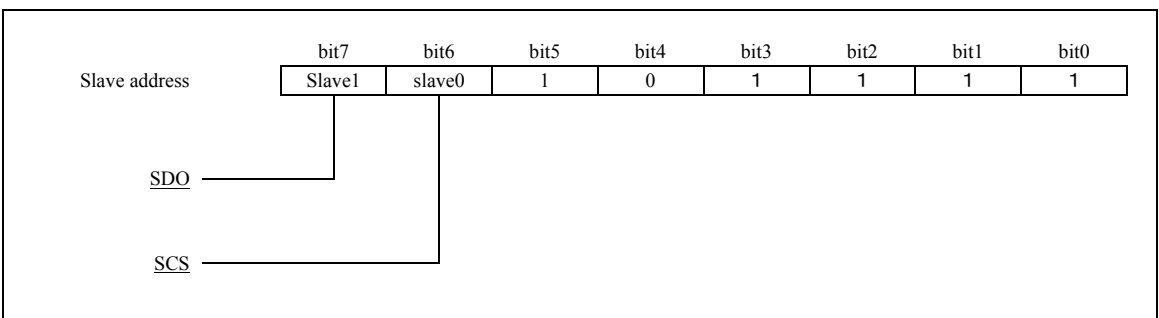
• I²C mode



Note:

Slave address can be set with the *sdo* and *scs* depending on your system configuration.
The *sdi_sda* and *scl_scl* terminals require pull-up resistors.
An external capacitor is required between AVDD and AGND.
Use of 10µF (≤ ±20%) and 4.7µF (≤ ±20%) aluminum electrolytic or tantalum capacitors (Recommended rated voltage: ≥16V), or 0.1µF (≤ ±20%) ceramic capacitors is recommended.
Capacitors indicated with * must be soldered on PCB

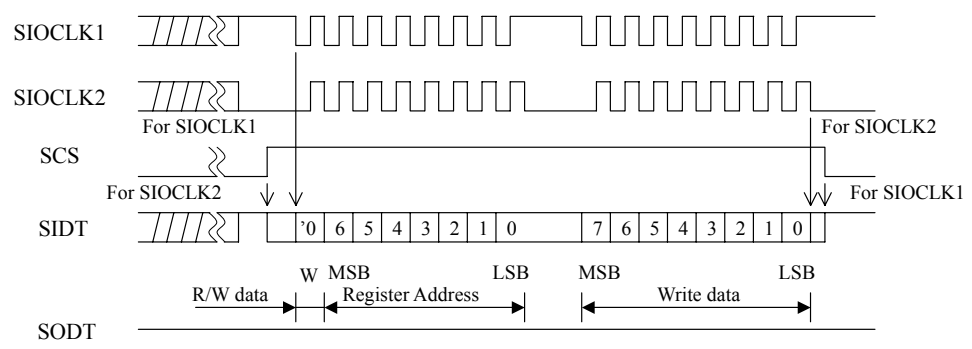
Setting maximum of four types of address can be set for I²C Slave address using the *scs* (slave address 0) and *sdo* (Slave address 1) in I²C mode.



Slave1 (sdo)	Slave0 (scs)	IRead Address (bit7~0)	Write Address (bit7~0)
0	0	2F	2E
0	1	6F	6E
1	0	AF	AE
1	1	EF	EE

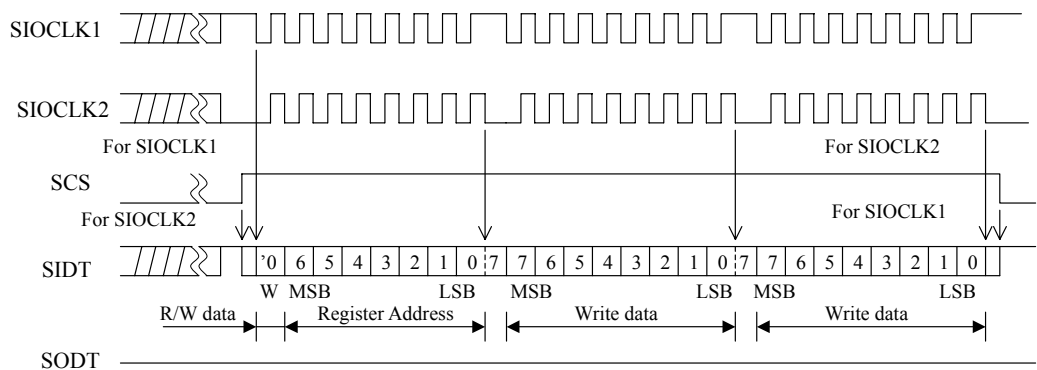
3.6 SPI interface

- Write sequence (1 byte)



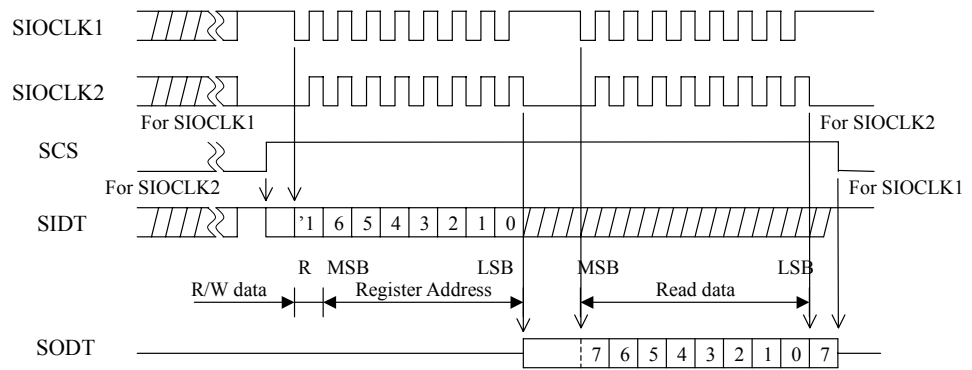
Both SIOCLK1(normally high) and SIOCLK2 (normally low) cases are supported.

- Write sequence (Continuous)



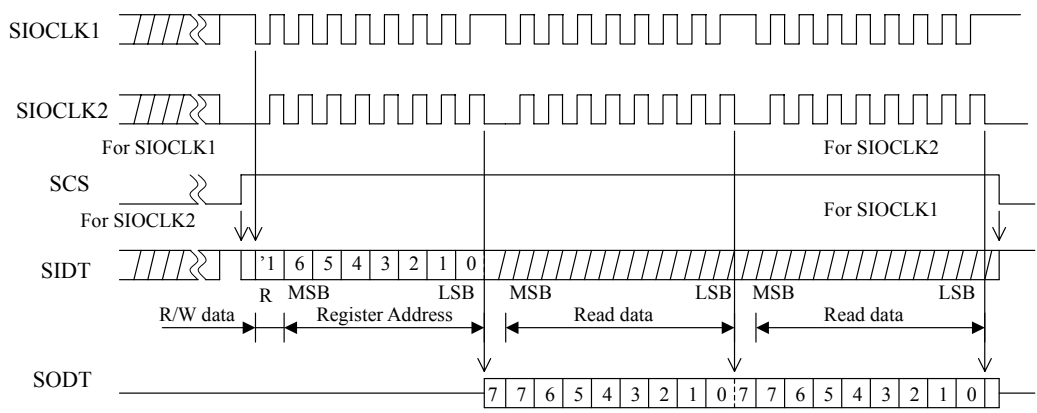
Both SIOCLK1(normally high) and SIOCLK2 (normally low) cases are supported.

- Read sequence (1 byte)



Both SIOCLK1(normally high) and SIOCLK2 (normally low) cases are supported.

• Read sequence (Continuous)



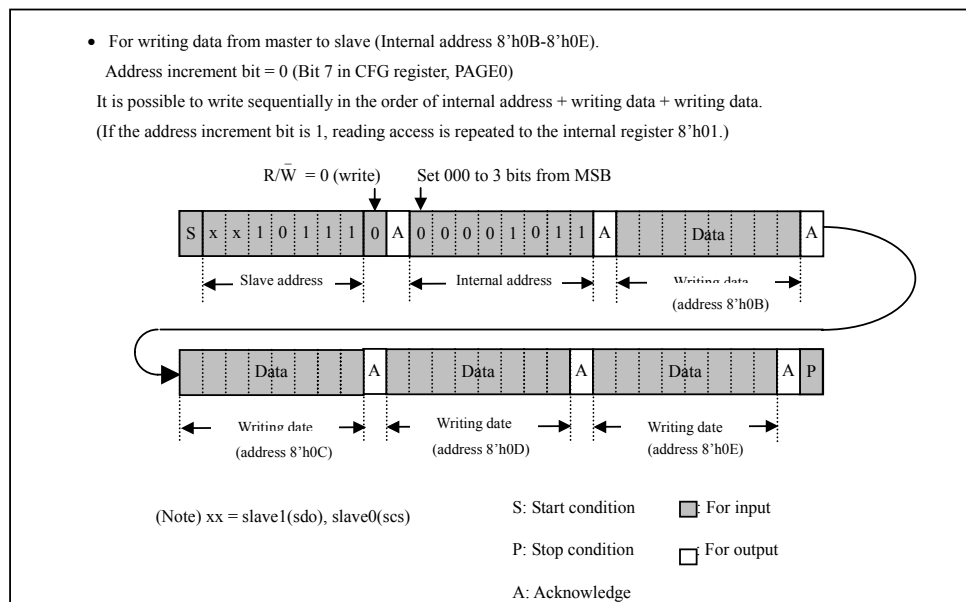
Both SIOCLK1(normally high) and SIOCLK2 (normally low) cases are supported.

3.7 I²C bus interface

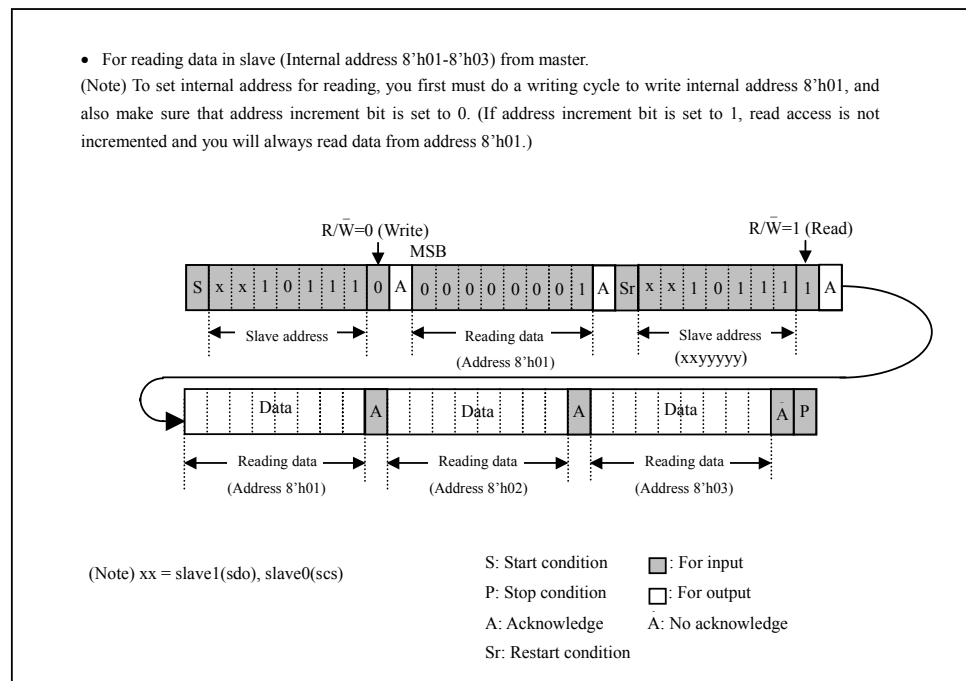
- Serial interface I²C mode (SPI/I²C pin = High)

Interface specification for the serial interface I²C mode is giveow.

(1) Write sequence



(2) Read sequence



4. REGISTERS

4.1 List of registers

4.1.1 Table of page 0 registers (For setup)

PAGE	Address	Register name	Description	bytes
0	01	DVRST	Software reset register	1
0	02	PDWN	Oscillator power down register	1
0	03	CTRL0	Operation mode setup register 0	1
0	04	RESERVE	Reserved	1
0	05	MODE0	Measurement mode setup register 0	1
0	06	MODE1	Measurement mode setup register 1	1
0	07	INTREQ	Interrupt request register	1
0	08	INTMSK	Interrupt mask setup register	1
0	09,0A	TMDL	Timer data setup register for automatic measurement	2
0	0B	RESERVE	Reserved	1
0	0C	CFG	Configuration register	1
0	0D	INTOTM	Automatic measurement interrupt output condition setup register	1
0	0E	GAAVE	Average rates setup register in automatic measurement mode	1
0	0F	GNAVE	Average rates setup register in acceleration normal measurement mode	1
0	10	RESERVE	Reserved	1
0	11,12	GDTCT0	Detection range threshold level setup register 0 in automatic measurement	2
0	13,14	GDTCT1	Detection range threshold level setup register 1 in automatic measurement	2
0	15	CPURDY	CPU ready register	1
0	1E	PAGE_SELECT	Page select register	1

Note:

RESERVE registers are not for use.

4.1.2 Table of page 1 registers (Result registers)

PAGE	Address	Register name	Description	bytes
1	01	STATUS	Operation status register	1
1	02,03	GAX	X-axis acceleration measurement result vector register in automatic measurement mode	2
1	04,05	GAY	Y-axis acceleration measurement result vector register in automatic measurement mode	2
1	06,07	GAZ	Z-axis acceleration measurement result vector register in automatic measurement mode	2
1	08,09	GASV	Composite acceleration measurement result register in automatic measurement mode	2
1	0A,0B	GNX	X-axis acceleration measurement result vector register in normal measurement mode	2
1	0C,0D	GNY	Y-axis acceleration measurement result vector register in normal measurement mode	2
1	0E,0F	GNZ	Z-axis acceleration measurement result vector register in normal measurement mode	2
1	10,11	GNSV	Composite acceleration measurement result register in normal measurement mode	2
1	12,13	PITCH	Pitch result register	2
1	14,15	ROLL	Roll result register	2
1	16,17	RESERVE	Reserved	2
1	18	RESERVE	Reserved	1
1	19,1A	TEMP	Temperature calculation result register	2
1	1E	PAGE_SELECT	Page select register	1

Note:

RESERVE registers are not for use.

4.1.3 Table of Page 6 registers (General purpose registers)

PAGE	Address	Register name	Description	bytes
6	01	HGR1	Command setup register	1
6	02-09	HRSV0-7	Setup register for each data	8
6	0A-11	RSV0-7	Reading register of each data	8

4.2 Register descriptions

4.2.1 Explanation of bits in registers

PAGE0: Registers for sensor control and interrupt control (For setup)

Address	Symbol	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
01H	DVRST	R/W	DVRST[7]	DVRST[6]	DVRST[5]	DVRST[4]	DVRST[3]	DVRST[2]	DVRST[1]	DVRST[0]
02H	PDWN	W	-	-	-	-	-	There is no influence in measurements. Both reading and writing are possible.		
03H	CTRL0	R/W	-	-	CTSTR	*	CGSTRNC			
04H	RESERVE	R/W	-	-	-	*	*	*	*	*
05H	MODE0	R/W	PDOF	RVOFF	TMPOFF	AGCON	MAUTO	-	GDET[1]	GDET[0]
06H	MODE1	R/W	-	-	3MOFF	-	-	-	AXIS[1]	AXIS[0]
07H	INTREQ	R	S7REQ	S6REQ	S5REQ	S4REQ	S3REQ	S2REQ	S1REQ	GAREQ

A “-” symbol in R/W represents the following actions:

- Writing will be ignored.
- 0 will be read in read mode.

4.2.2 Table of page 0 registers

PAGE0: Registers for sensor control and interrupt control (For setup)

Address	Symbol	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
01H	DVRST	R/W	DVRST[7]	DVRST[6]	DVRST[5]	DVRST[4]	DVRST[3]	DVRST[2]	DVRST[1]	DVRST[0]
02H	PDWN	W	-	-	-	-	-	-	-	PDWN
03H	CTRL0	R/W	-	-	CTSTR	*	CGSTRNC	CGSTRC	*	CGAUTO
04H	RESERVE	R/W	-	-	-	*	*	*	*	*
05H	MODE0	R/W	PDOFF	RVOFF	TMPOFF	AGCON	MAUTO	-	GDET[1]	GDET[0]
06H	MODE1	R/W	-	-	3MOFF	-	-	-	AXIS[1]	AXIS[0]
07H	INTREQ	R	-	-	S5REQ	-	S3REQ	S2REQ	-	GAREQ
08H	INTMSK	R/W	*	*	S5MSK	*	S3MSK	S2MSK	*	GAMSK
09H	TMDL	R/W	TMD[7]	TMD[6]	TMD[5]	TMD[4]	TMD[3]	TMD[2]	TMD[1]	TMD[0]
0AH	TMDH	R/W	TMD[15]	TMD[14]	TMD[13]	TMD[12]	TMD[11]	TMD[10]	TMD[9]	TMD[8]
0BH	RESERVE	R/W	-	-	-	-	-	*	*	*
0CH	CFG	R/W	REGMD	SPI3M	-	SDOCFG	INT1EN	INTLVL	INT1CFG	INT0CFG
0DH	INTOTM	R/W	NMR[3]	NMR[2]	NMR[1]	NMR[0]	DNM[3]	DNM[2]	DNM[1]	DNM[0]
0EH	GAAVE	R/W	-	-	-	-	-	GAAVE [2]	GAAVE [1]	GAAVE [0]
0FH	GNAVE	R/W	-	-	-	-	-	GNAVE [2]	GNAVE [1]	GNAVE [0]
10H	RESERVE	R/W	-	-	-	-	-	*	*	*
11H	GDTCT0L	R/W	GDTCT0[7]	GDTCT0[6]	GDTCT0[5]	GDTCT0[4]	GDTCT0[3]	GDTCT0[2]	GDTCT0[1]	GDTCT0[0]
12H	GDTCT0H	R/W	-	-	GDTCT0[13]	GDTCT0[12]	GDTCT0[11]	GDTCT0[10]	GDTCT0[9]	GDTCT0[8]
13H	GDTCT1L	R/W	GDTCT1[7]	GDTCT1[6]	GDTCT1[5]	GDTCT1[4]	GDTCT1[3]	GDTCT1[2]	GDTCT1[1]	GDTCT1[0]
14H	GDTCT1H	R/W	-	-	GDTCT1[13]	GDTCT1[12]	GDTCT1[11]	GDTCT1[10]	GDTCT1[9]	GDTCT1[8]
15H	CPURDY	R	-	-	-	-	-	-	-	READY
1EH	PGSEL	R/W	-	-	-	-	-	PGSEL[2]	PGSEL[1]	PGSEL[0]

4.2.3 Table of page 1 registers

PAGE1: Calculation result registers

Address	Symbol	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
01H	STATUS	R	-	-	-	-	-	-	ASTS	STS
02H	GAXL	R	GAX[7]	GAX[6]	GAX[5]	GAX[4]	GAX[3]	GAX[2]	GAX[1]	GAX[0]
03H	GAXH	R	GAX[13]	GAX[13]	GAX[13]	GAX[12]	GAX[11]	GAX[10]	GAX[9]	GAX[8]
04H	GAYL	R	GAY[7]	GAY[6]	GAY[5]	GAY[4]	GAY[3]	GAY[2]	GAY[1]	GAY[0]
05H	GAYH	R	GAY[13]	GAY[13]	GAY[13]	GAY[12]	GAY[11]	GAY[10]	GAY[9]	GAY[8]
06H	GAZL	R	GAZ[7]	GAZ[6]	GAZ[5]	GAZ[4]	GAZ[3]	GAZ[2]	GAZ[1]	GAZ[0]
07H	GAZH	R	GAZ[13]	GAZ[13]	GAZ[13]	GAZ[12]	GAZ[11]	GAZ[10]	GAZ[9]	GAZ[8]
08H	GASVL	R	GASV[7]	GASV[6]	GASV[5]	GASV[4]	GASV[3]	GASV[2]	GASV[1]	GASV[0]
09H	GASVH	R	-	-	GASV[13]	GASV[12]	GASV[11]	GASV[10]	GASV[9]	GASV[8]
0AH	GNXL	R	GX[7]	GX[6]	GX[5]	GX[4]	GX[3]	GX[2]	GX[1]	GX[0]
0BH	GNXH	R	GX[13]	GX[13]	GX[13]	GX[12]	GX[11]	GX[10]	GX[9]	GX[8]
0CH	GNYL	R	GY[7]	GY[6]	GY[5]	GY[4]	GY[3]	GY[2]	GY[1]	GY[0]
0DH	GNYH	R	GY[13]	GY[13]	GY[13]	GY[12]	GY[11]	GY[10]	GY[9]	GY[8]
0EH	GNZL	R	GZ[7]	GZ[6]	GZ[5]	GZ[4]	GZ[3]	GZ[2]	GZ[1]	GZ[0]
0FH	GNZH	R	GZ[13]	GZ[13]	GZ[13]	GZ[12]	GZ[11]	GZ[10]	GZ[9]	GZ[8]
10H	GNSVL	R	GNSV [7]	GNSV [6]	GNSV [5]	GNSV [4]	GNSV [3]	GNSV [2]	GNSV [1]	GNSV [0]
11H	GNSVH	R	-	-	GNSV [13]	GNSV [12]	GNSV [11]	GNSV [10]	GNSV [9]	GNSV [8]
12H	PITCHL	R	PITCH[7]	PITCH[6]	PITCH[5]	PITCH[4]	PITCH[3]	PITCH[2]	PITCH[1]	PITCH[0]
13H	PITCHH	R	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[8]
14H	ROLLL	R	ROLL[7]	ROLL[6]	ROLL[5]	ROLL[4]	ROLL[3]	ROLL[2]	ROLL[1]	ROLL[0]
15H	ROLLH	R	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[8]
16H	RESERVE	R	-	-	-	-	-	-	-	-
17H	RESERVE	R	-	-	-	-	-	-	-	-
18H	RESERVE	R	-	-	-	-	-	-	-	-
19H	TEMPL	R	TEMP[7]	TEMP[6]	TEMP[5]	TEMP[4]	TEMP[3]	TEMP[2]	TEMP[1]	TEMP[0]
1AH	TEMPH	R	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]
1EH	PGSEL	R/W	-	-	-	-	-	PGSEL[2]	PGSEL[1]	PGSEL[0]

4.2.4 Table of page 6 registers

PAGE6: General purpose registers

ADDR	Symbol	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
01H	HGRI	R/W	HGRI[7]	HGRI[6]	HGRI[5]	HGRI[4]	HGRI[3]	HGRI[2]	HGRI[1]	HGRI[0]
02H	HRSV0	R/W	HRSV0[7]	HRSV0[6]	HRSV0[5]	HRSV0[4]	HRSV0[3]	HRSV0[2]	HRSV0[1]	HRSV0[0]
03H	HRSV1	R/W	HRSV1[7]	HRSV1[6]	HRSV1[5]	HRSV1[4]	HRSV1[3]	HRSV1[2]	HRSV1[1]	HRSV1[0]
04H	HRSV2	R/W	HRSV2[7]	HRSV2[6]	HRSV2[5]	HRSV2[4]	HRSV2[3]	HRSV2[2]	HRSV2[1]	HRSV2[0]
05H	HRSV3	R/W	HRSV3[7]	HRSV3[6]	HRSV3[5]	HRSV3[4]	HRSV3[3]	HRSV3[2]	HRSV3[1]	HRSV3[0]
06H	HRSV4	R/W	HRSV4[7]	HRSV4[6]	HRSV4[5]	HRSV4[4]	HRSV4[3]	HRSV4[2]	HRSV4[1]	HRSV4[0]
07H	HRSV5	R/W	HRSV5[7]	HRSV5[6]	HRSV5[5]	HRSV5[4]	HRSV5[3]	HRSV5[2]	HRSV5[1]	HRSV5[0]
08H	HRSV6	R/W	HRSV6[7]	HRSV6[6]	HRSV6[5]	HRSV6[4]	HRSV6[3]	HRSV6[2]	HRSV6[1]	HRSV6[0]
09H	HRSV7	R/W	HRSV7[7]	HRSV7[6]	HRSV7[5]	HRSV7[4]	HRSV7[3]	HRSV7[2]	HRSV7[1]	HRSV7[0]
0AH	RSV0	R	RSV0[7]	RSV0[6]	RSV0[5]	RSV0[4]	RSV0[3]	RSV0[2]	RSV0[1]	RSV0[0]
0BH	RSV1	R	RSV1[7]	RSV1[6]	RSV1[5]	RSV1[4]	RSV1[3]	RSV1[2]	RSV1[1]	RSV1[0]
0CH	RSV2	R	RSV2[7]	RSV2[6]	RSV2[5]	RSV2[4]	RSV2[3]	RSV2[2]	RSV2[1]	RSV2[0]
0DH	RSV3	R	RSV3[7]	RSV3[6]	RSV3[5]	RSV3[4]	RSV3[3]	RSV3[2]	RSV3[1]	RSV3[0]
0EH	RSV4	R	RSV4[7]	RSV4[6]	RSV4[5]	RSV4[4]	RSV4[3]	RSV4[2]	RSV4[1]	RSV4[0]
0FH	RSV5	R	RSV5[7]	RSV5[6]	RSV5[5]	RSV5[4]	RSV5[3]	RSV5[2]	RSV5[1]	RSV5[0]
10H	RSV6	R	RSV6[7]	RSV6[6]	RSV6[5]	RSV6[4]	RSV6[3]	RSV6[2]	RSV6[1]	RSV6[0]
11H	RSV7	R	RSV7[7]	RSV7[6]	RSV7[5]	RSV7[4]	RSV7[3]	RSV7[2]	RSV7[1]	RSV7[0]
1EH	PGSEL	R/W	-	-	-	-	-	PGSEL[2]	PGSEL[1]	PGSEL[0]

4.3 Details of registers

4.3.1 Page 0 registers

4.3.1.1 Device reset register (PAGE0 / 01h): DVRST

The device reset register DVRST initiates a software reset.

All blocks except for the serial interface are reset by writing 3CH into the register.

Writing C3H into the register disables software reset.

Note: Hardware reset must be performed upon power up.

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DVRST (01H)	DVRST[7]	DVRST[6]	DVRST[5]	DVRST[4]	DVRST[3]	DVRST[2]	DVRST[1]	DVRST[0]
Default 00H (R/W)								

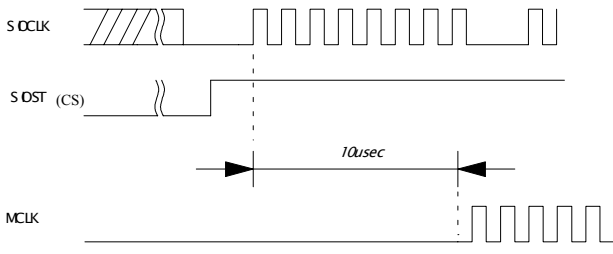
4.3.1.2 Power-down register for oscillator (PAGE0 / 02h): PDWN

This register is used to stop the oscillator. Writing 1 stops the oscillator circuit. Resuming from power-down state takes place either by accessing from HOST-CPU with SPI or inputting the same slave address in I²C. Stop the oscillator after all measurements have finished. Stopping the current operation is not guaranteed if stopping the oscillator in the middle of a measurement. Current consumption in the power down is typically 5 μ A.

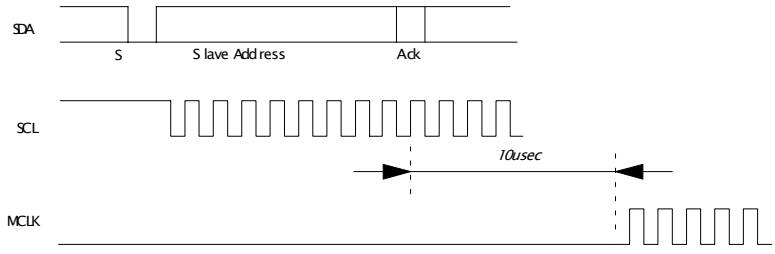
PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PDWN (02H)	-	-	-	-	-	-	-	PDWN
Default 00H (W)								

Note: Wake-up time, 10 μ s. (Max.)

• SPI Communication:



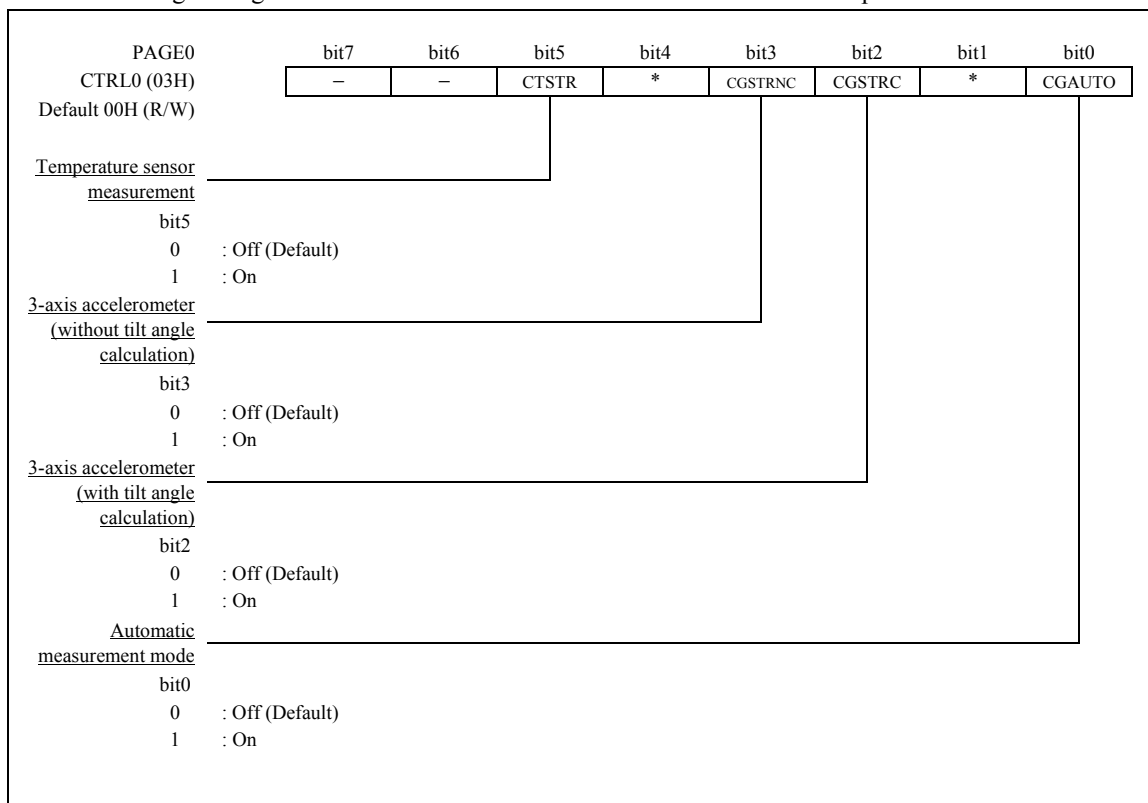
• I²C communication:



4.3.1.3 Operation mode control register 0 (PAGE0 / 03h): CTRL0

The CTRL0 is the register to configure operation modes of the ML8953A.

Note that accessing the register is not allowed until the current measurement is completed.



bit5: CTSTR

Writing 1 to this bit performs a temperature measurement. Once the measurement is finished, the register is cleared.

bit3: CGSTRNC

Writing 1 to this bit performs an acceleration measurement. Once the measurement is finished, the register is cleared.

Acceleration measurement: Tri-axis continuous measurement mode (Automatic continuous internal measurement of X, Y, and Z axes) and axis selectable measurement mode.

Please refer to the MODE1 (06H) for the axis selectable measurement mode.

bit2: CGSTRC

Writing 1 to this bit performs an acceleration measurement, then tilt angles (pitch and roll) are calculated. After completing the measurement, the register is cleared.

Acceleration measurement: Tri-axis continuous measurement mode (Automatic continuous internal measurement of X, Y, and Z axes).

bit0: CGAUTO

Writing 1 to this bit performs automatic acceleration measurement. Setting 0 into the CGAUT ends the automatic measurement mode.

Automatic measurement mode performs tri-axis continuous mode (automatic continuous internal measurement X, Y and Z axes) along with temperature measurement and temperature compensation.

Note:

- Setting bits 2, 3 and 5 simultaneously is prohibited. If this setting is made, 0XF0 will be set into the INT_REQ (PAGE0-07) automatically without affecting the operation.
- Accessing the register is not allowed until the current measurement is finished. If an instruction to start the next measurement (changing setting to the CTRL0) is set during the current measurement, 0X0F is set into the INT_REQ (PAGE0-07) by issuing an interrupt from the INT pin after completing the current measurement.

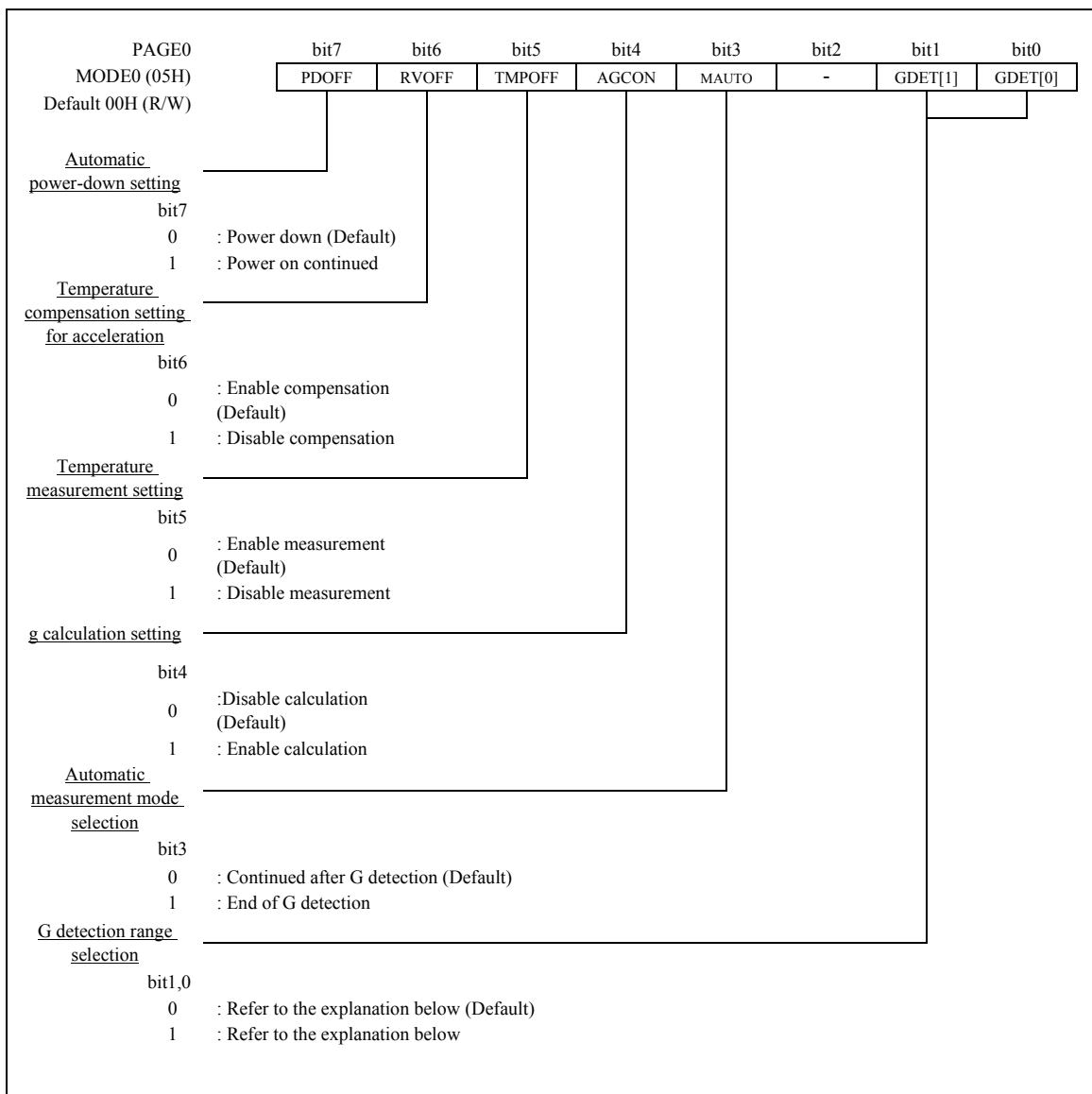
It is not necessary to reset when an error occurs. The normal measurement is performed if the prohibited actions written above are not set.

Explanation of operation modes

Function	Description
Temperature sensor measurement	Only measures temperature
3-axis accelerometer (Without tilt angle compensation)	After measuring acceleration, acceleration on each axis and composite vector of X, Y and Z axes are calculated.
3-axis accelerometer (With tilt angle compensation)	After measuring the accelerometer (without tilt angle calculation) written above, pitch and roll are calculated afterwards.
Automatic measurement mode	<p>Temperature (for temperature compensation) and the accelerometer (without tilt calculation) measurements are performed at a previously set interval. An interrupt signal is issued to the host controller when the composite acceleration of three axes exceeds a previously set threshold level (considered as g detection).</p> <p>The g detection conditions should be set using the following registers. GDTCT0/1 (11 ~ 14H in PAGE0), INTOTM (0DH in PAGE0), MODE0 (05H in PAGE0) [1:0].</p> <p>Pitch and roll will be calculated after automatic measurement is finished by setting 1 in bit 4 of the MODE 0 (05H in PAGE0).</p>

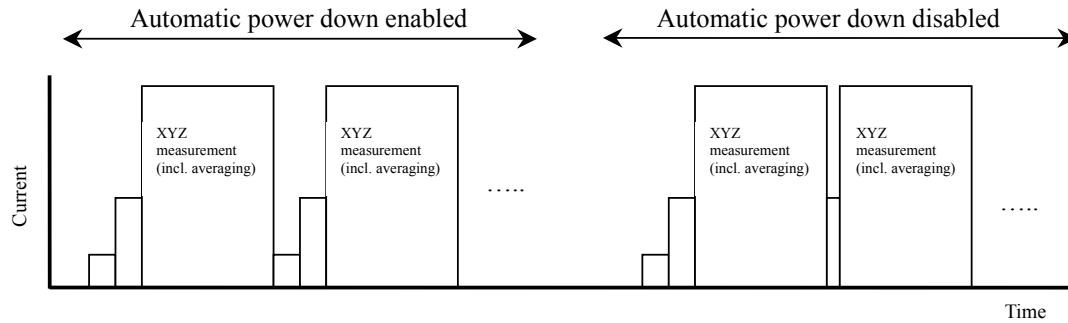
4.3.1.4 Sensor measurement mode register 0 (PAGE0 / 05h): MODE0

The MODE0 is the register for setting the acceleration measurement mode.



bit7: PDOFF

Writing 1 to this bit disables the automatic power down of VREF, BIAS, AD, DA and GS blocks after completing measurement. By default, the above blocks go to a power-down mode automatically after measurement to save power consumption. Set 1 to this register if high speed measurement is performed. Power applied in VREF/BIAS/AD/DA/GS blocks is not turned off every time the high speed measurement finishes.



bit6: RVOFF

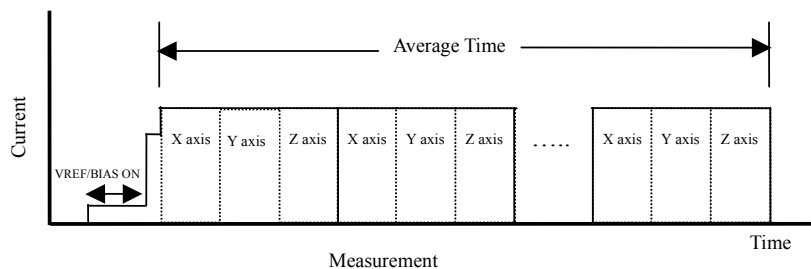
Writing 1 to this bit disables the temperature compensation for the accelerometer. This function is not effective in the automatic measurement mode.

bit5: TMPOFF

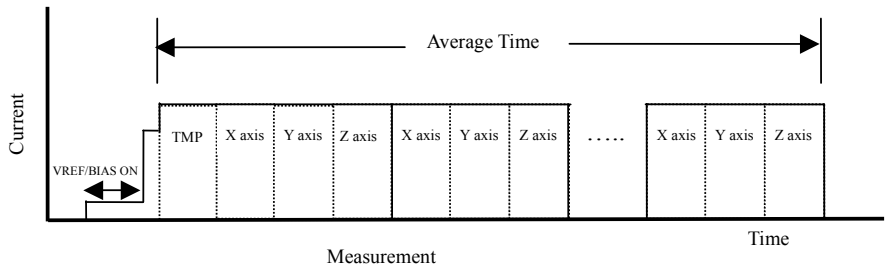
Writing 1 to this bit disables the temperature measurement, which is performed once before acceleration measurement starts. This function is not effective in the automatic measurement mode.

If temperature compensation is enabled without temperature measurement, compensation is made using the previously measured temperature. Please note if the temperature measurement is not performed at all, compensation is made with the value of 0. In this setting, temperature calculation in °C is not performed although TEMP measurement is enabled. In order to make a temperature calculation in °C, read TEMP registers (19H and 1AH in PAGE 1) if temperature measurement is performed by setting 1 on the bit 5 of CTRL0 (03H in PAGE 0).

Temperature setting disabled (Setting 1 in the TMPOFF bit of the MODE0 register)



Temperature setting enabled (Setting 0 in the TEMPOFF bit of the MODE0 register)



bit4: AGCON

By writing 1 to this bit, pitch and roll angles are calculated after acceleration measurement is completed in the automatic measurement mode (Only effective in automatic measurement mode). In this case, measurement time and power consumption increase due to pitch and roll angle calculations.

bit3: MAUTO

By writing 0 to this bit, the automatic measurement continues even after g is detected. In order to stop the automatic measurement mode, setting 0 to the CGAUT in the CTRL is required.

By writing 1 to this bit, the automatic measurement mode terminates once g has been detected. The CGAUTO bit in the CTRL is cleared.

The g detection conditions are determined by the settings in the GDTCT0/1 (11 to 14H in PAGE 0), INTOTM (0DH in PAGE 0), and MODE0 (06H in PAGE 0) [1:0].

(bit1, bit0): GDET[1:0]

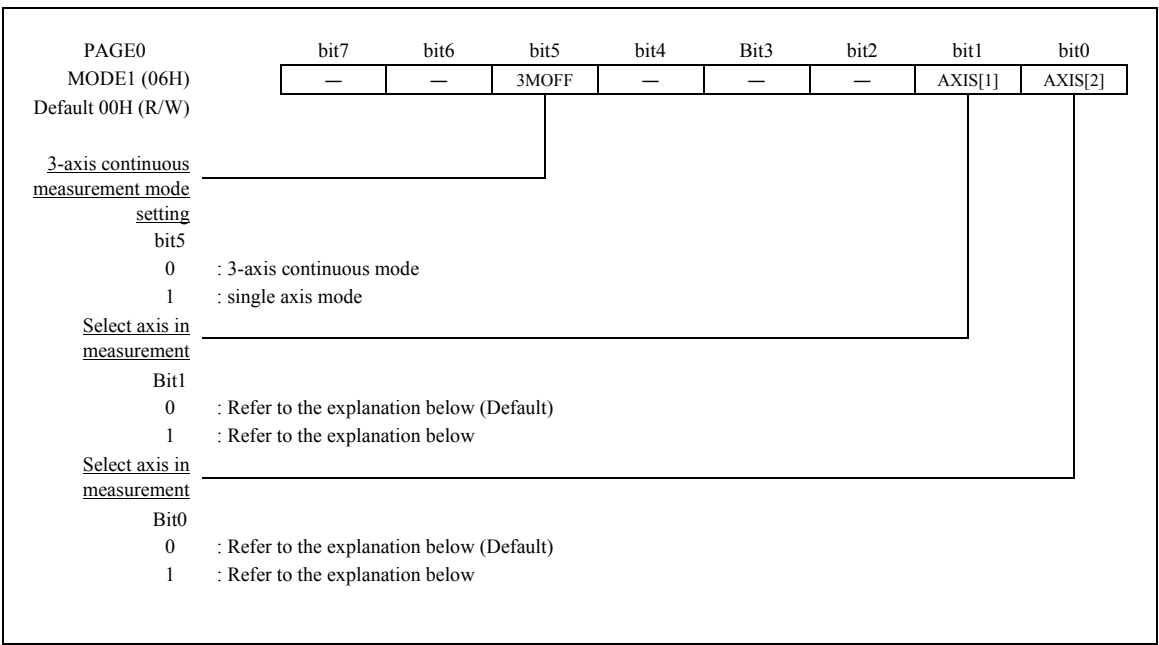
Threshold level in g detection is specified. The value in the GDTCT0/1(11 to 14H in PAGE 0) is used as a threshold value. Comparison between the composite value of acceleration (square root of sum of the squared value of the acceleration on the three axes) and value in the GDTCT1 and 0 is made.

The interrupt signal is issued when the following condition is met.

Setting		Detection range (g)	Setting example
GDET[1]	GDET[0]		
0	0	$GDTCT1 \leq G \leq GDTCT0$ (Default)	$0 \leq G \leq 0.4$
0	1	$GDTCT1 \geq G, G \geq GDTCT0$	$0.4 \geq G, G \geq 1.5$
1	0	$G \geq GDTCT0$	$G \geq 2.5$

4.3.1.5 Sensor measurement mode register 1 (PAGE0 / 06h): MODE1

The MODE1 is the register to select measurement modes for the accelerometer.



bit5:3MOFF

Setting this bit to 1 disables the 3-axis continuous mode and enables the measurement of a desired axis. The 3MOFF affects the acceleration measurement mode. If single axis mode is selected, set 1 to only bit3 of the CTRL0.

Note that temperature is not measured in the single-axis-measurement mode. If temperature measurement is needed, set 1 to the bit 5 (CTSTR) in the CTRL0 register. Temperature compensation will be made with the temperature each time acceleration measurement finishes in this mode.

- Configuration of (bit1, bit2):AXIS[1:0]
- (1, 1) : Z-axis selection
 - (1, 0) : Y-axis selection
 - (0, 1) : X-axis selection
 - (0, 0) : Reference-axis selection (Default)

Note:

The reference axis is the output when the internal reference voltage, which is 1 volt, is applied to both inputs of the differential amplifier in the LSI.

4.3.1.6 Sensor interrupt request register (PAGE0 / 07h): INTREQ

The INTREQ is a read-only register provided to notify cause of interrupt.

Reading 1 from the specified bit in the INTREQ clears the bit.

Note that if an error occurs, F0 is set in the INTREQ register.

When the following errors occur, F0 is set to the INTREQ register.

- I) More than 2 bits are set in bits 2, 3 and 5 of the CTRL0 simultaneously.
- II) A command is set in the middle of a measurement.
- III) A 1 is set to bit 1 or bit 4 in the CTRO.
- IV) In accessing to general purpose register, command password is wrong.
- V) In adjusting accelerometer offset, output of the horizontal axes is 0.4g or greater.

0x00H will be set after the INTREQ is read.

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
INTREQ (07H)	—	—	S5REQ	—	S3REQ	S2REQ	—	GAREQ
Default 00H (R)								
<u>Temperature sensor interrupt</u>								
bit5								
0								
1								
<u>3-axis accelerometer (No tilt angle calculation) interrupt</u>								
bit3								
0								
1								
<u>3-axis accelerometer (Including tilt angle calculation) interrupt</u>								
bit2								
0								
1								
<u>g detection interrupt</u>								
bit0								
0								
1								

bit5 : S5REQ (TREQ)

Interrupt is requested when temperature measurement finishes. A 1 is set once the temperature measurement finishes regardless of the setting in the INTMSK (PAGE0-08H) register.

bit3 : S3REQ (GREQ)

Interrupt is requested when acceleration measurement (no tilt calculation) finishes. A 1 is set when the measurement and g calculation finish regardless of the setting in the INTMSK (PAGE 0-08H) register.

bit2 : S2REQ (GCREQ)

Interrupt is requested when acceleration measurement (including tilt calculation) finishes. A 1 is set when g, pitch and roll calculations finish regardless of the setting in the INTMSK (PAGE 0-08H) register.

bit0 : GAREQ

In the automatic measurement mode, interrupt is requested once g detection condition is met. A 1 is set once the condition is met regardless of the setting in the INTMSK (PAGE 0-08H) register.

About restriction of reading INTREQ

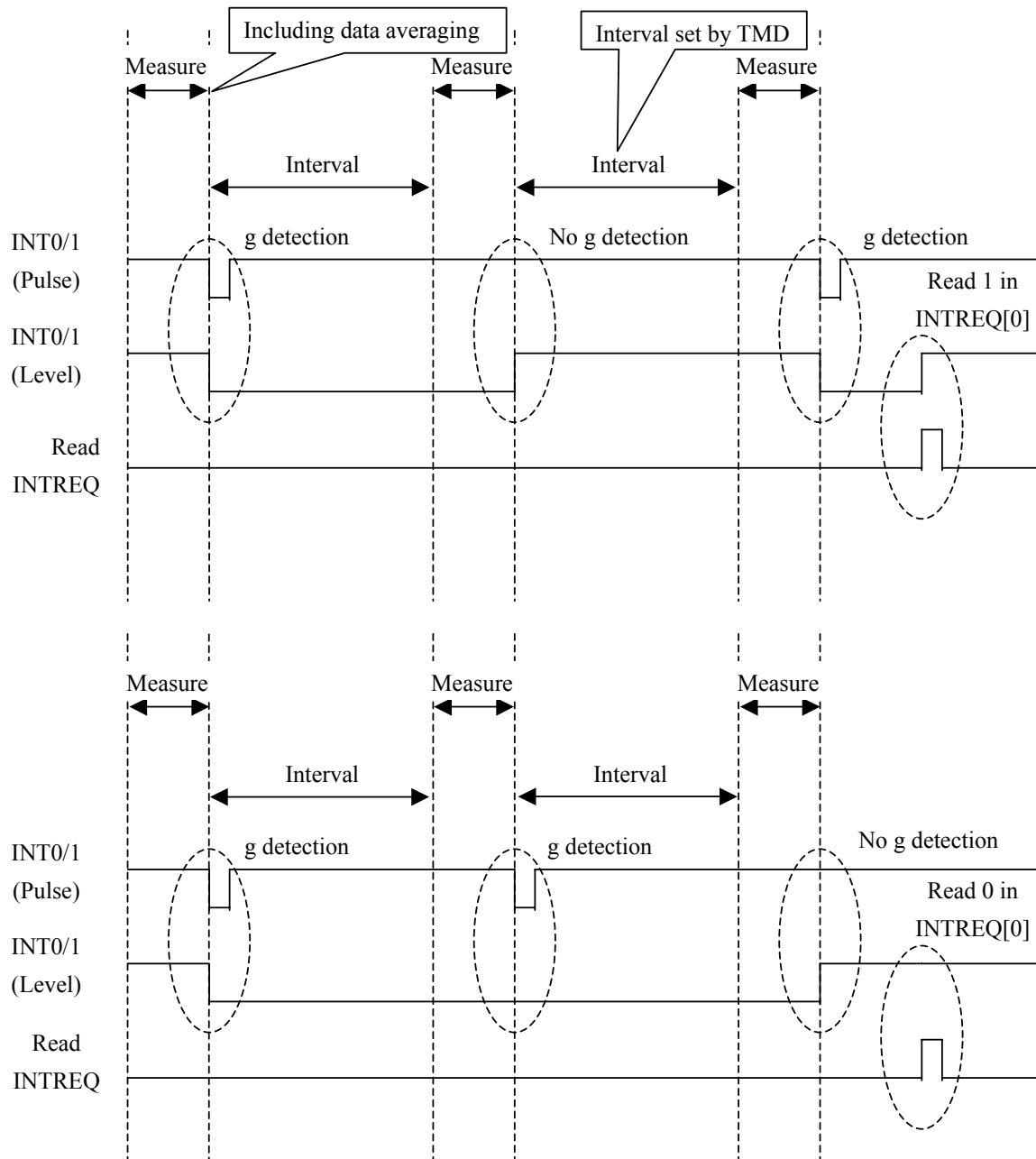
The following restrictions are applied to the INTREQ:

- Polling INTREQ is prohibited because the interrupt request signal may be cleared.
- INTREQ must be read only after an interrupt occurs.

It is possible to check the internal conditions of the STATUS register by polling.

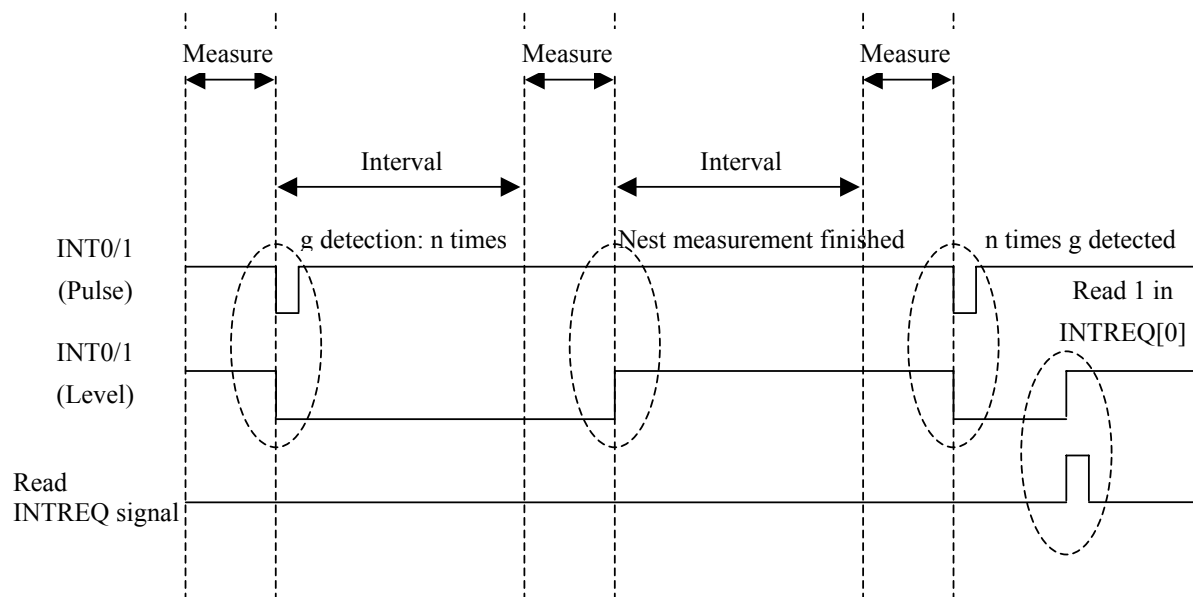
The following chart shows interrupt request flags and timing diagrams of the interrupt signals associated with the INT 0/INT 1.

- For g detection interrupt (Detection count setting condition: $1/m$, where m is total number of measurements)



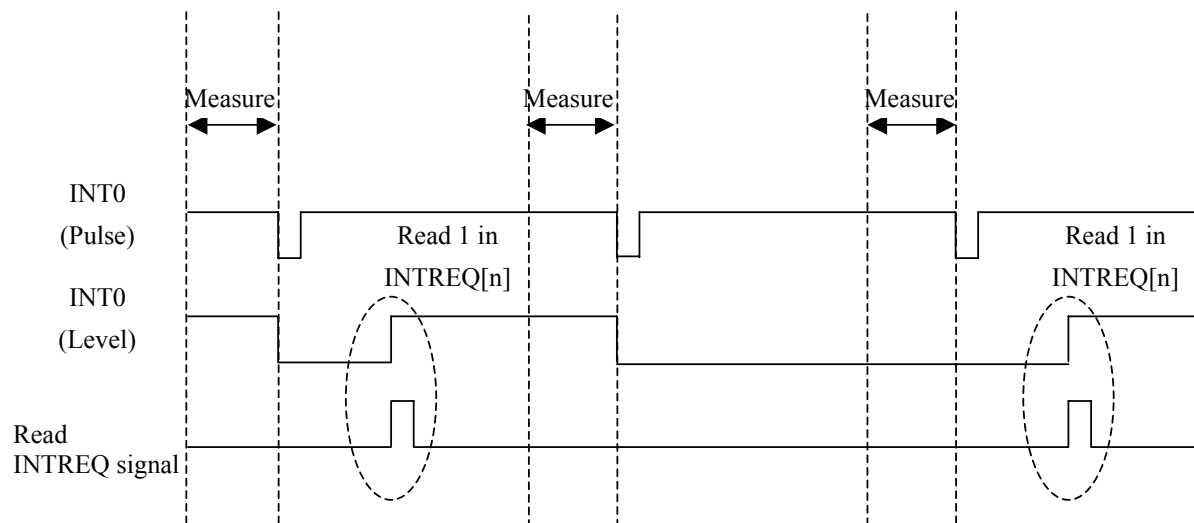
Note that the timing diagram above is designed for when the interrupt masking is disabled. No signal is driven at the INT0/1 upon masking the interrupt. However, the INTREQ read value is generated when an interrupt occurs whatever the setting in the interrupt mask is.

- For g detection interrupt (Detection count setting condition: n/m , where n is the number of detections)



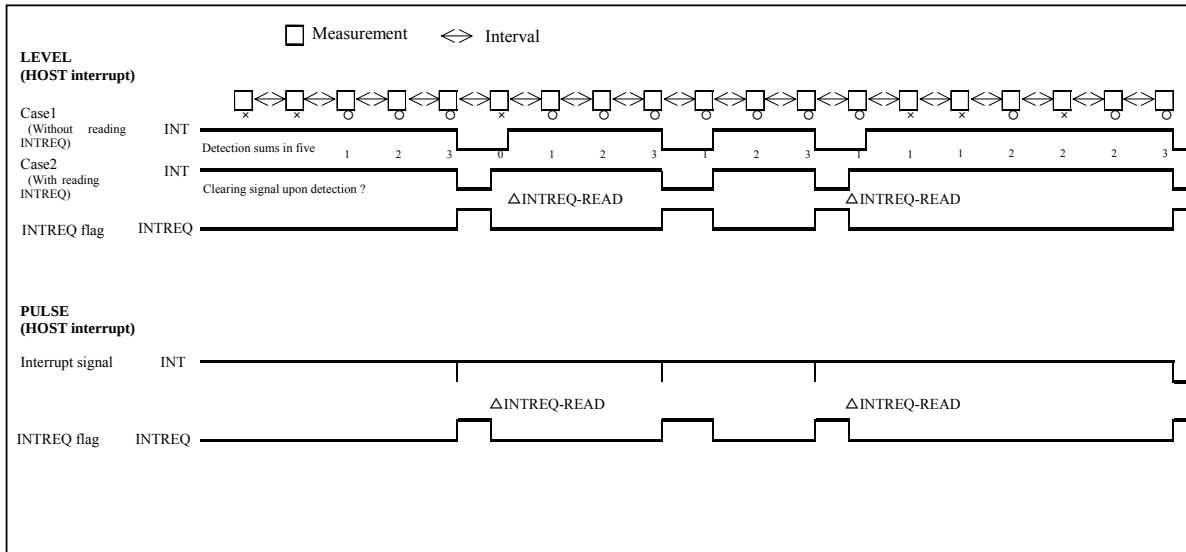
Note that if INTREQ is not read after g is detected n times, the level interrupt is cleared in the next measurement. In this case, the INTREQ itself is not cleared.

- For interrupt other than g detection (Acceleration and temperature measurements)



Note that the timing diagram above is designed for when the interrupt masking is disabled. No signal is driven at the INT0 upon masking the interrupt. However, the INTREQ read value is generated when an interrupt occurs whatever the setting in the interrupt mask is.

Example of g detection interrupt (Detection threshold: 3/5)



4.3.1.7 Sensor interrupt mask setting register (PAGE0 / 08h): INTMSK

The INTMSK is the register for enabling or disabling interrupt operation.

(Settings for enabling or disabling interrupt output from the INT0/1 pins.)

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
INTMSK (08H)	—	—	S5MSK	—	S3MSK	S2MSK	—	GAMSK
Default FFH (R/W)								
<u>Temperature sensor</u>								
<u>measurement</u>								
<u>interrupt mask</u>								
bit5								
0								
: Allowed								
1								
: Mask (Default)								
<u>3-axis accelerometer</u>								
<u>interrupt mask (No</u>								
<u>tilt angle calculation)</u>								
bit3								
0								
: Allowed								
1								
: Mask (Default)								
<u>3-axis accelerometer</u>								
<u>interrupt mask</u>								
<u>(Including tilt</u>								
<u>angle calculation)</u>								
bit2								
0								
: Allowed								
1								
: Mask (Default)								
<u>g detection interrupt</u>								
<u>mask</u>								
bit0								
0								
: Allowed								
1								
: Mask (Default)								

bit5: S5MSK (TMSK)

-Temperature measurement termination interrupt mask-

The interrupt is masked by writing 1. If an interrupt is detected while the interrupt was masked, the interrupt will be issued right after the mask has been disabled.

bit3: S3MSK (GMSK)

-Acceleration measurement (no tilt angle calculation) termination interrupt mask-

The interrupt is masked by writing 1. If an interrupt is detected while the interrupt was masked, the interrupt will be issued right after the mask has been disabled.

bit2: S2MSK (GCMSK)

-Acceleration measurement (including tilt angle calculation) termination interrupt mask-

The interrupt is masked by writing 1. If an interrupt is detected while the interrupt was masked, the interrupt will be issued right after the mask has been disabled.

bit0: GMSK

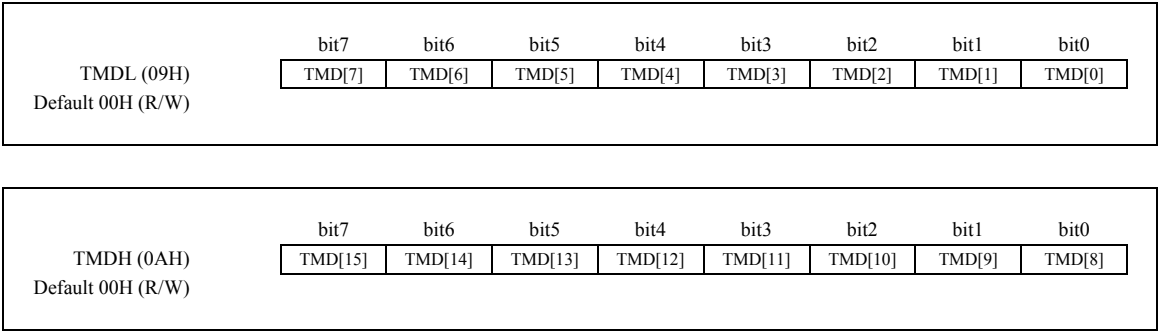
-g detection interrupt mask-

The interrupt is masked by writing 1. If an interrupt is detected while the interrupt was masked, the interrupt will be issued right after the mask has been disabled.

4.3.1.8 Timer data register for automatic measurement mode (PAGE0 / 09~0Ah): TMD

The TMD is the timer data register for setting interval time in the automatic measurement mode.
In the automatic measurement mode, when the value set in the TMD and the value in the internal counter become the same, the acceleration measurement starts after power-up in the analog circuit section* is completed. The internal counter is reset, and it re-starts counting-up after the acceleration measurement has been cometed.

 * Note that power-up time in the analog circuit section is stabilization time of VREF/BIAS/AD/DA/GS blocks.



Setting range: 1 to FFFFH (Setting 0 is not allowed.)
Interval time (in seconds) = (1/internal clock frequency) x 2048 x TMD

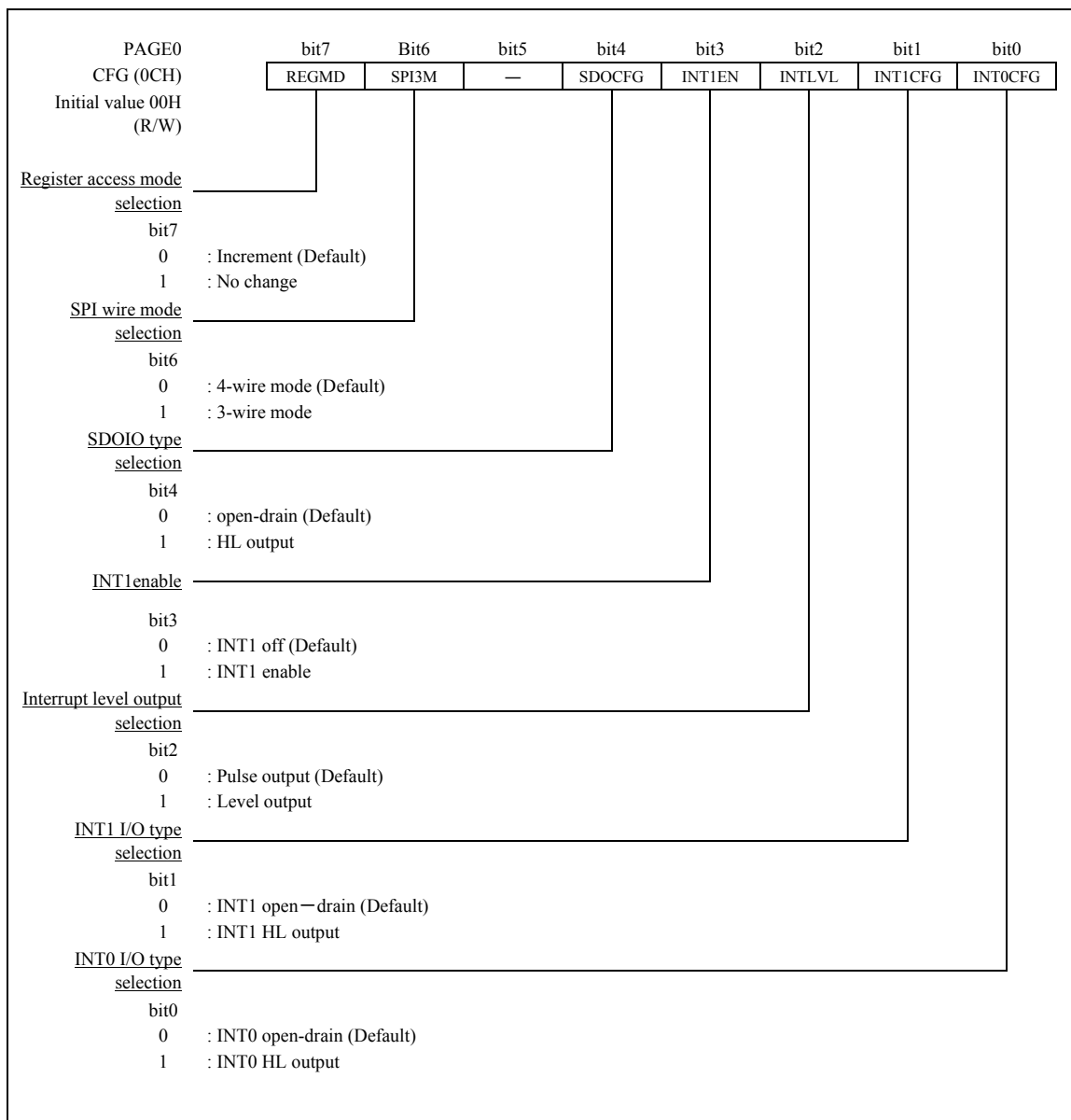
- Standard setting time
Internal clock: 6.2 MHz (Typ.)
Clock divider ratio: 2048 (Fixed)
For example:

Setting 1000 in TMD, the interval time can be calculated as:

Interval time = (1/6.2 MHz) x 2048 x 1000 ≈ 330 ms.

4.3.1.9 Configuration register (PAGE0 / 0Ch): CFG

The CFG is the register to select register access mode, open-drain I/O mode and interrupt mode.



bit7: REGMD

The register access mode in the serial interface (SPI/I²C) is determined. By writing 0, the internal address is incremented by 1 each time a 1-byte data is transmitted/received. By writing 1, the address does not change.

bit6: SPI3M

The register access mode in the SPI interface is determined. Writing 0 sets the serial interface to 4-wire mode. Writing 1 activates the 3-wire mode. The *sdi_sda* pin is used for transferring and receiving data.

bit4: SDOCFG

The SDO pin outputs H/L by writing 1 to this bit. The open-drain mode is set by writing 0.

bit3: INT1EN

By writing 1 to this bit, the INT1 pin outputs only the g detection interrupt. Other types of interrupt are issued from the INT0 pin.

By writing 0, all interrupts are issued from the INT0. The maskable register needs to have a permission to interrupt.

bit2: INTLVL

By writing 1 to this bit, the interrupt signal from the INT0/INT1 becomes a level output. By writing 0, the interrupt signal from INT0/INT1 becomes a pulse Output.

bit1: INT1CFG

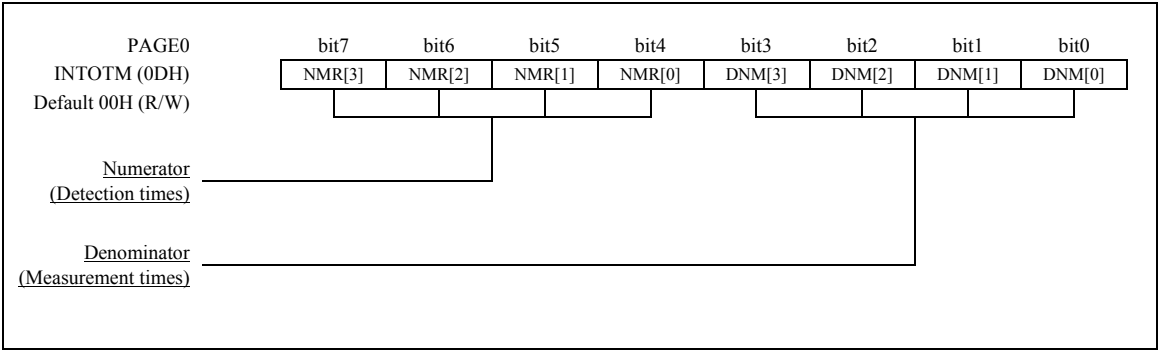
The INT1 pin outputs H/L by writing 1 to this. The open-drain mode is set by writing 0.

bit0:INT0CFG

The INT0 pin outputs H/L by writing 1 to this bit. The open-drain mode is set by writing 0.

4.3.1.10 g detection interrupt output condition settings (PAGE0 / 0Dh): INTOTM

The INTOTM is the register to set the g detection interrupt output conditions.



bit7-4: NMR[3:0]

This register is used to set the number of g detection times. The number of times to be set is from 0 to 15.

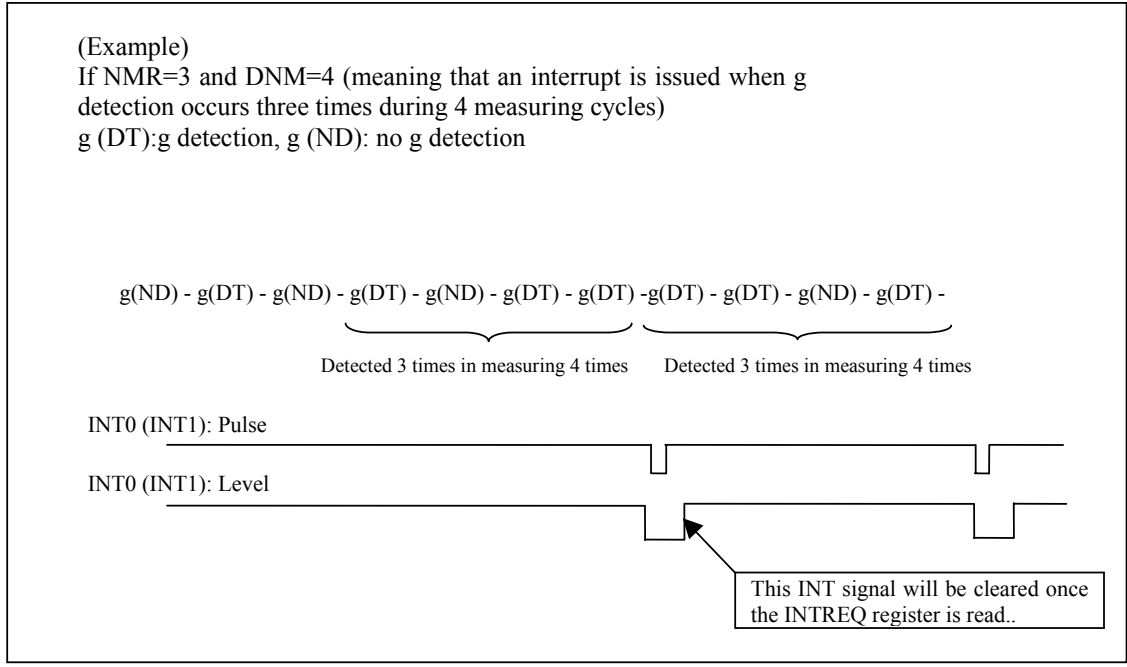
bit3-0: DNM[3:0]

This register is used to set the number of all measurements. The number of times to be set is from 0 to 15.

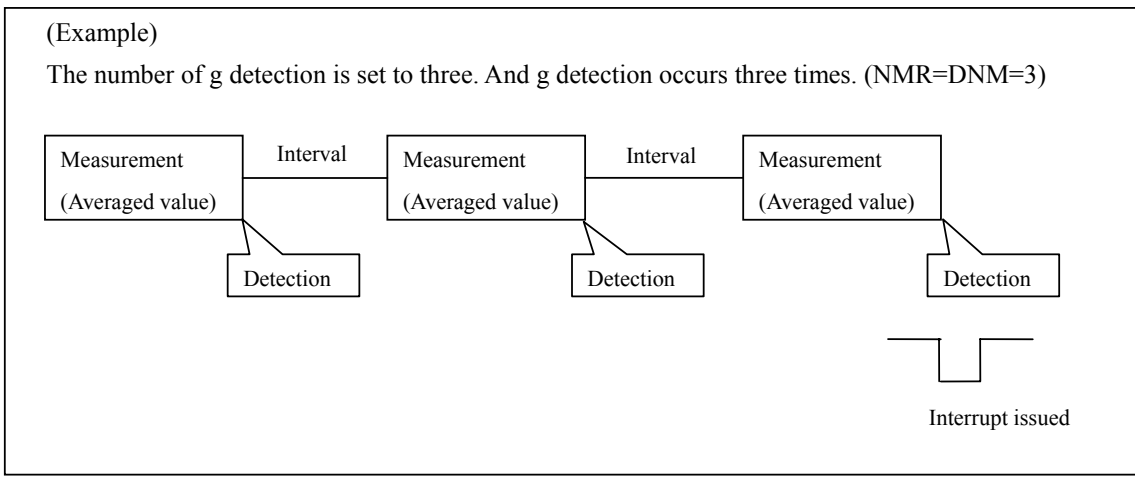
Note that if 00H is set to the INTOTM, the setting is dealt as 11H setting internally.

The INTOTM is the register to determine how many g detection counts are needed to issue the interrupt. The DNM is the total number of measurements. The NMR is the number of counts, which is incremented each time g detection occurs. It is necessary to have the condition of $NMR \leq DNM$ to operate appropriately. When $NMR =$

DNM = 0, NMR = DNM = 1 or NMR = 1, the interrupt signal is issued when g detection occurs once. The setting of a NMR>DNM condition is prohibited. If g detection occurs sequentially, and the number of counts set in the NMR is reached, the interrupt signal is issued at the last g detection occurred. At this event, the detection count starts from 0.



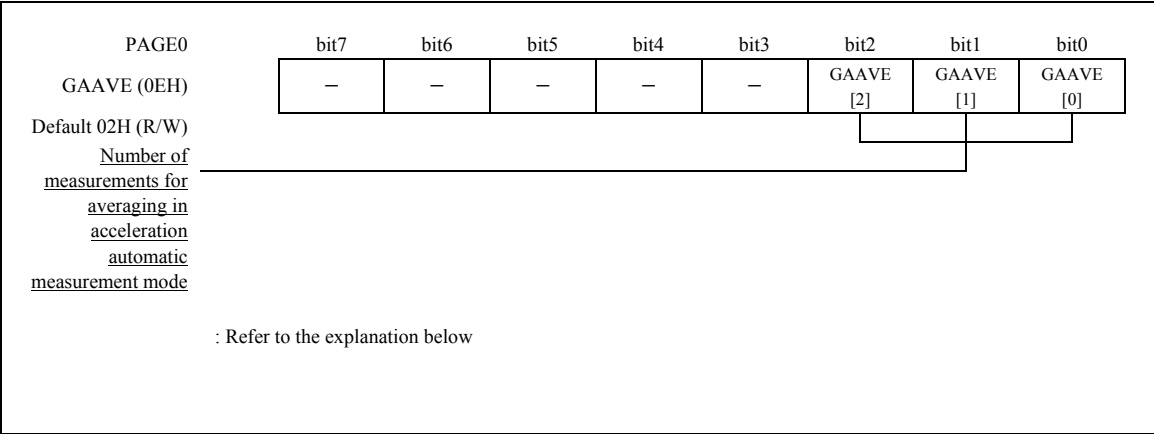
g detection interrupt output conditions



Relationship between the number of measurements in average and interrupt signal output in g detection.

4.3.1.11 Data averaging in automatic acceleration measurement mode (PAGE0 / 0EH): GAAVE

The GAAVE is the register to set the number of times data is measured to calculate an average in the automatic measurement.



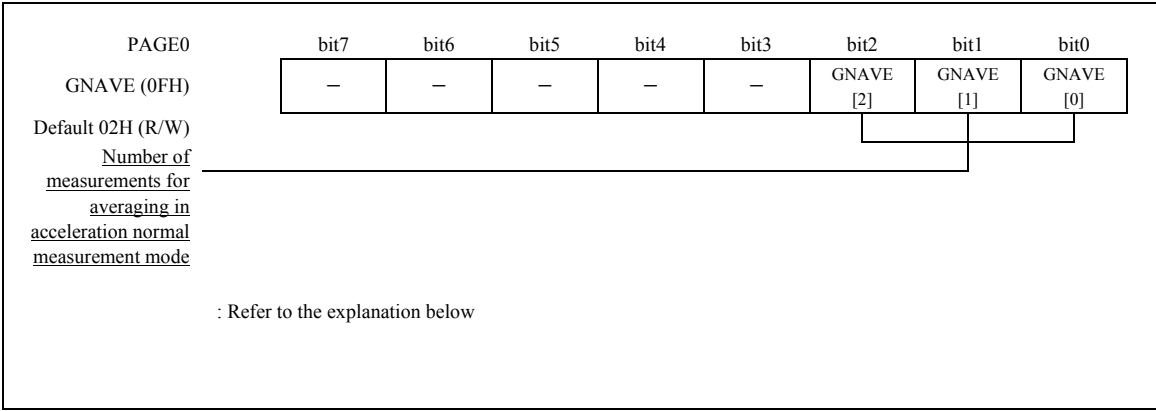
(bit2,bit1,bit0):GAAVE [2:0]

The number of times data is measured to calculate an average can be selected from the Table.

Setting			Number of measurements in average (Times)
GAAVE2[2]	GAAVE2[1]	GAAVE2[0]	
0	0	0	1
0	0	1	2
0	1	0	4 (Default)
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

4.3.1.12 Data averaging in normal acceleration measurement mode (PAGE0 / 0Fh): GNAVE

The GNAVE is the register to set the number of times data is measured to calculate an average in the normal acceleration measurement.



(bit2,bit1,bit0):GNAVE [2:0]

The number of times data is measured to calculate an average in normal acceleration measurement can be selected from the Table.

Setting			Number of measurements in average (Times)
GNAVE2[2]	GNAVE2[1]	GNAVE2[0]	
0	0	0	1
0	0	1	2
0	1	0	4 (Default)
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

4.3.1.13 g detection threshold level setting register (PAGE0 / 11~14h): GDTCT0/1

The GDTCT0/1 are the registers to change the g detection threshold level set in the GDET of MODE0 register.

The interrupt signal is issued to the host controller when the total acceleration, $\sqrt{(x^2 + y^2 + z^2)}$, exceeds the threshold level set in the GDTCT0/1 under the g detection condition.

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GDTCT0L (11H)	GDTCT0[7]	GDTCT0[6]	GDTCT0[5]	GDTCT0[4]	GDTCT0[3]	GDTCT0[2]	GDTCT0[1]	GDTCT0[0]
Default 00H (RW)								

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GDTCT0H (12H)	—	—	GDTCT0[13]	GDTCT0[12]	GDTCT0[11]	GDTCT0[10]	GDTCT0[9]	GDTCT0[8]
Default 00H (RW)								

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GDTCT1L (13H)	GDTCT1[7]	GDTCT1[6]	GDTCT1[5]	GDTCT1[4]	GDTCT1[3]	GDTCT1[2]	GDTCT1[1]	GDTCT1[0]
Default 00H (RW)								

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GDTCT1H (14H)	—	—	GDTCT1[13]	GDTCT1[12]	GDTCT1[11]	GDTCT1[10]	GDTCT1[9]	GDTCT1[8]
Default 00H (RW)								

This setting must be made in g detection (automatic) measurement because the default is 00H.

GDTCT0/1 [9:0] is fractional part. It is possible to set from 0 to 16383 (equivalent to 15.999g) in the register but operation only performs from 0 to 3072 (equivalent to 3g) correctly.

Note: In practice, if outputs of GAX, GAY and GAZ are between ± 3 and ± 5 , the maximum total acceleration becomes $8.660g (\sqrt{(5g)^2 + (5g)^2 + (5g)^2})$. It means that the sensor will not perform correctly with a greater value than 8.660g as a threshold level.

Example setting

For setting 0.4g: Set 410 ($0.4 \times 1024 \approx 409$) (it may contain some rounding error)

For setting 1.5g: Set 1536 ($1.5 \times 1024 \approx 1536$) (it may contain some rounding error)

4.3.1.14 CPU ready register (PAGE0 / 15h): CPURDY

The CPURDY is the register to notify the completion of internal controller’s initialization.

Measuring sensor should be performed after confirming that 1 is set in the READY bit.

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CPURDY (15H)	—	—	—	—	—	—	—	READY
Default 00H (R)								

bit0: READY

0: Initialization in progress

1: Initialization completed

Note: Rise time of the READY bit, initialization time, is typically 2ms (Max. 4ms) after reset is disabled.

4.3.1.15 Register page selection register (1Eh): PGSEL

The PGSEL is a special register to select the register page. This register allows reading or writing from any page.

The bit2 to 7 must be set to 0.

PAGEn	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PGSEL (1EH)	0	0	0	0	0	PGSEL[2]	PGSEL[1]	PGSEL[0]
Default 00H (R/W)								

	Bit2	bit0	Bit1
PAGE0	0	0	0
PAGE1	0	0	1
PAGE6	1	1	0

4.3.2 Page 1 register

4.3.2.1 Status register (PAGE1 / 01h): STATUS

The STATUS register contains the status of measurement.

PAGE1	Bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
STATUS (01H)	—	—	—	—	—	—	ASTS	STS
Default 00H (R)								
<u>Status for automatic measurement</u>								
bit0								
0	: No measurement / Under interval (Default)							
1	: Under acceleration measurement							
<u>Status</u>								
bit0								
0	: No measurement (Default)							
1	: Under measurement							

bit1: ASTS

A 1 indicates that the accelerometer is under measurement in the automatic measurement mode.

A 0 indicates that the accelerometer is not under measurement, that is, current status is the interval between measurements.

bit0: STS

A 1 indicates that the measurement is progressing in all measurement modes except the automatic measurement mode. A 0 indicates that the measurement is in a hold state or completed.

4.3.2.2 g vector register for automatic measurement mode (PAGE1 / 02~07h): GAX/Y/Z

The GAX, GAY and GAZ read registers contain acceleration vectors in the automatic measurement mode. The values internally calculated in g are placed in the registers.

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GAXL (02H)	GAX[7]	GAX[6]	GAX[5]	GAX[4]	GAX[3]	GAX[2]	GAX[1]	GAX[0]
Default 00H (R)								

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GAXH (03H)	GAX[13]	GAX[13]	GAX[13]	GAX[12]	GAX[11]	GAX[10]	GAX[9]	GAX[8]
Default 00H (R)								

The GAX[9:0] is the fractional part, GAX[12:10] is the integer part, and GAX[13] is the sign in GAX[13:0]. This

also applies to the GAYL/H and GAZL/H.

GAX/Y/Z[13] = 0 and 1 represent positive and negative acceleration, respectively.

Setting example and decimal conversion

- 1.234 (10) is expressed as 0000 0100 1111 0000 (2) equivalent to 1264 (10).
Dividing this by 1024 equals to 1.234375 (including rounding error)
- -1.234 (10) is expressed as 1111 1011 0001 0000 (2) equivalent to 64272 (10).
Inverting each bit, adding 1 and dividing by 1024 equal to -1.234375 (including rounding error)

4.3.2.3 Acceleration composite vector register for automatic measurement mode (PAGE1 / 08~09h): GASV

The GASV read register contains an internally calculated result of acceleration composite vector in the automatic measurement mode.

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GASVL (08H)	GASV[7]	GASV[6]	GASV[5]	GASV[4]	GASV[3]	GASV[2]	GASV[1]	GASV[0]
Default 00H (R)								

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GASVH (09H)	—	—	GASV[13]	GASV[12]	GASV[11]	GASV[10]	GASV[9]	GASV[8]
Default 00H (R)								

The GASV [13:10] and GASV [9:0] in the GASV are the integer part and fractional part, respectively.

In practice, if outputs of GAX, GAY and GAZ are between ± 3 and ± 5 , the maximum total acceleration becomes $8.660g (\sqrt{(5g)^2 + (5g)^2 + (5g)^2})$.

Setting example and decimal conversion

- 1.234 (10) is expressed as 0000 0100 1111 0000 (2) equivalent to 12 (10).
Dividing this by 1024 equals to 1.234375 (including rounding error)

4.3.2.4 g vector register for normal measurement mode (PAGE1 / 0A~0Fh): GNX/Y/Z

The GNX, GNY and GNZ read registers contain acceleration vector in the normal measurement mode. The values internally calculated in g are placed in the registers

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GNXL (0AH)	GNX[7]	GNX [6]	GNX [5]	GNX [4]	GNX [3]	GNX [2]	GNX [1]	GNX [0]
Default 00H (R)								

PAGE0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GNXH (0BH)	GNX [13]	GNX [13]	GNX [13]	GNX [12]	GNX [11]	GNX [10]	GNX [9]	GNX [8]
Default 00H (R)								

The GNX[9:0] is the fractional part, GNX[12:10] is the integer part, and GNX[13] is the sign in GNX[13:0]. This also applies to the GNYL/H and GNZL/H.

GNX/Y/Z[13] = 0 and 1 represent positive and negative acceleration, respectively

Please refer to the example given in the g vector register for automatic measurement mode section, GAX/Y/Z, for decimal conversion.

4.3.2.5 Acceleration composite vector register for normal measurement mode (PAGE1 / 10~11h): GNSV

The GNSV read register contains an internally calculated result of acceleration composite vector in the automatic measurement mode.

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GNSVL (10H)	GNSV[7]	GNSV [6]	GNSV [5]	GNSV [4]	GNSV [3]	GNSV [2]	GNSV [1]	GNSV [0]
Default 00H (R)								

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
GNSVH (11H)			GNSV [13]	GNSV [12]	GNSV [11]	GNSV [10]	GNSV [9]	GNSV [8]
Default 00H (R)								

The GNSV [13:10] and GNSV [9:0] in the GNSV are integer part and fractional part, respectively.

Please refer to the example given in the Acceleration composite vector register for automatic measurement mode (PAGE1 / 01h), GASV, for decimal conversion.

4.3.2.6 Tilt angle result register (PAGE1 / 12~15h): PITCH, ROLL

The PITCH and ROLL read registers contain calculated tilt angles.

PAGE1	Bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PITCHL (12H)	PITCH[7]	PITCH[6]	PITCH[5]	PITCH[4]	PITCH[3]	PITCH[2]	PITCH[1]	PITCH[0]
Default 00H (R)								

PAGE1	Bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PITCHH (13H)	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[9]	PITCH[8]
Default 00H (R)								

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ROLL (14H)	ROLL[7]	ROLL[6]	ROLL[5]	ROLL[4]	ROLL[3]	ROLL[2]	ROLL[1]	ROLL[0]
Default 00H (R)								

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ROLLH (15H)	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[9]	ROLL[8]
Default 00H (R)								

PITCH: Pitch is defined as y-axis rotation around x-axis. In other words, pitch is considered when the Pin 1 goes up (+direction) and down (- direction).

ROLL: Roll is defined as x-axis rotation around y-axis. In other words, roll is considered when the Pin 6 goes up (+ direction) and down (- direction).

PITCH(ROLL)[0] is fractional part, PITCH(ROLL) [1]-[8] is integer part, and PITCH(ROLL) [9] is sign part.

PITCH(ROLL)[9] = 0 and 1 represent positive and negative angle, respectively

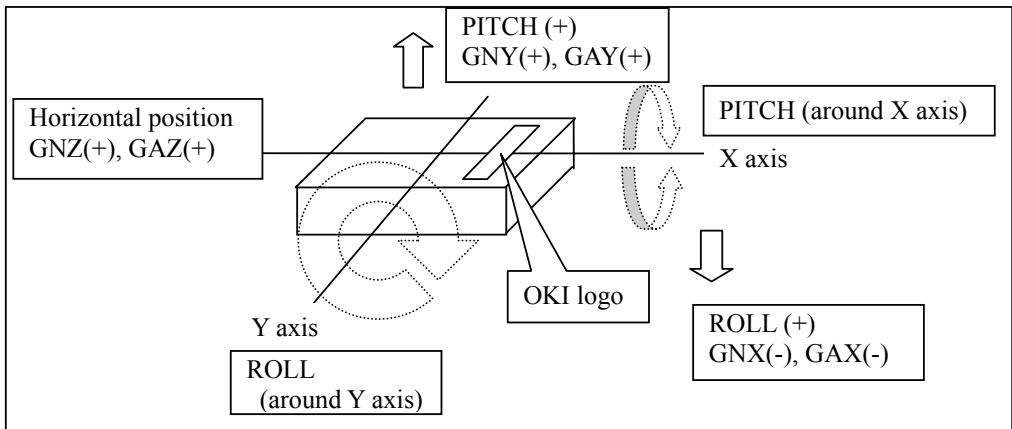
Note that the total acceleration is beyond the range between 0.5 and 2.0g, the registers are not updated. That is, angle calculation stops because proper calculation will not be made beyond the given ranges.

The representation range is $\pm 180^\circ$ by 0.5° step. (2's complement).

Example settings:

For $+180^\circ$: 0x0168 will be set.

For -180° : 0xFE98 will be set.



Pitch and roll directions, and their respective outputs

4.3.2.7 Temperature calculation result storage register (PAGE1 / 19~1Ah): TEMP

The TEMP read register contains an internally calculated temperature. The temperature measurement result is stored into this register only when temperature measurement is performed, that is, writing 1 in bit 5 of CTRL0 (PAGE0-03H).

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TEMPL (19H)	TEMP[7]	TEMP[6]	TEMP[5]	TEMP[4]	TEMP[3]	TEMP[2]	TEMP[1]	TEMP[0]
Default 00H (R)								

PAGE1	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TEMPH (1AH)	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]	TEMP[8]
Default 00H (R)								

The TEMP[0] is fractional part , TEMP[1:7] is integer part, and TEMP[8] in the TEMP is sign part. The range to be expressed is between -20 and 70°C.

TEMP[8] = 0 and 1 represent positive and negative temperatures, respectively.

The temperature sensor measures the temperature of inside the sensor. Temperature difference may be observed depending on external conditions.

Setting example and decimal conversion

- 25.5°C (10) is expressed as 0000 0000 0011 0011 (2) in the register, equivalent to 51 (10).
The 51 as a result of temperature measurement should be divided by 2, which equals to 25.5.
- -10.5°C (10) is expressed as 1111 1111 1110 1011 (2) in the register, equivalent to 65515 (10).
Inverting each bit, adding 1 and dividing by 2 equal to -10.5.

4.3.3 Page 6 registers

The page 6 registers are provided for offset adjustment. Descriptions of their use are given in section 5.6.

4.3.3.1 General purpose registers 0 (PAGE6 / 01~09h)

The HGRI and HRSV0-7 are general purpose registers, which will be used to read and write.

PAGE6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HGRI(01H)	HGRI[7]	HGRI[6]	HGRI[5]	HGRI[4]	HGRI[3]	HGRI[2]	HGRI[1]	HGRI[0]
Default 00H (R/W)								

PAGE6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HRSVn(02H-09H)	HRSVn[7]	HRSVn[6]	HRSVn[5]	HRSVn[4]	HRSVn[3]	HRSVn[2]	HRSVn[1]	HRSVn[0]
Default 00H (R/W)								

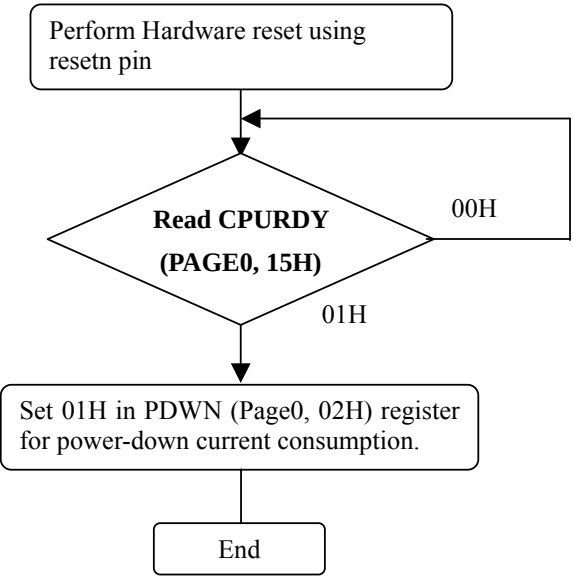
4.3.3.2 General purpose registers 1 (PAGE6 / 0A~11h)

The RSV0-7 are general purpose registers, which will be used to read from a host controller.

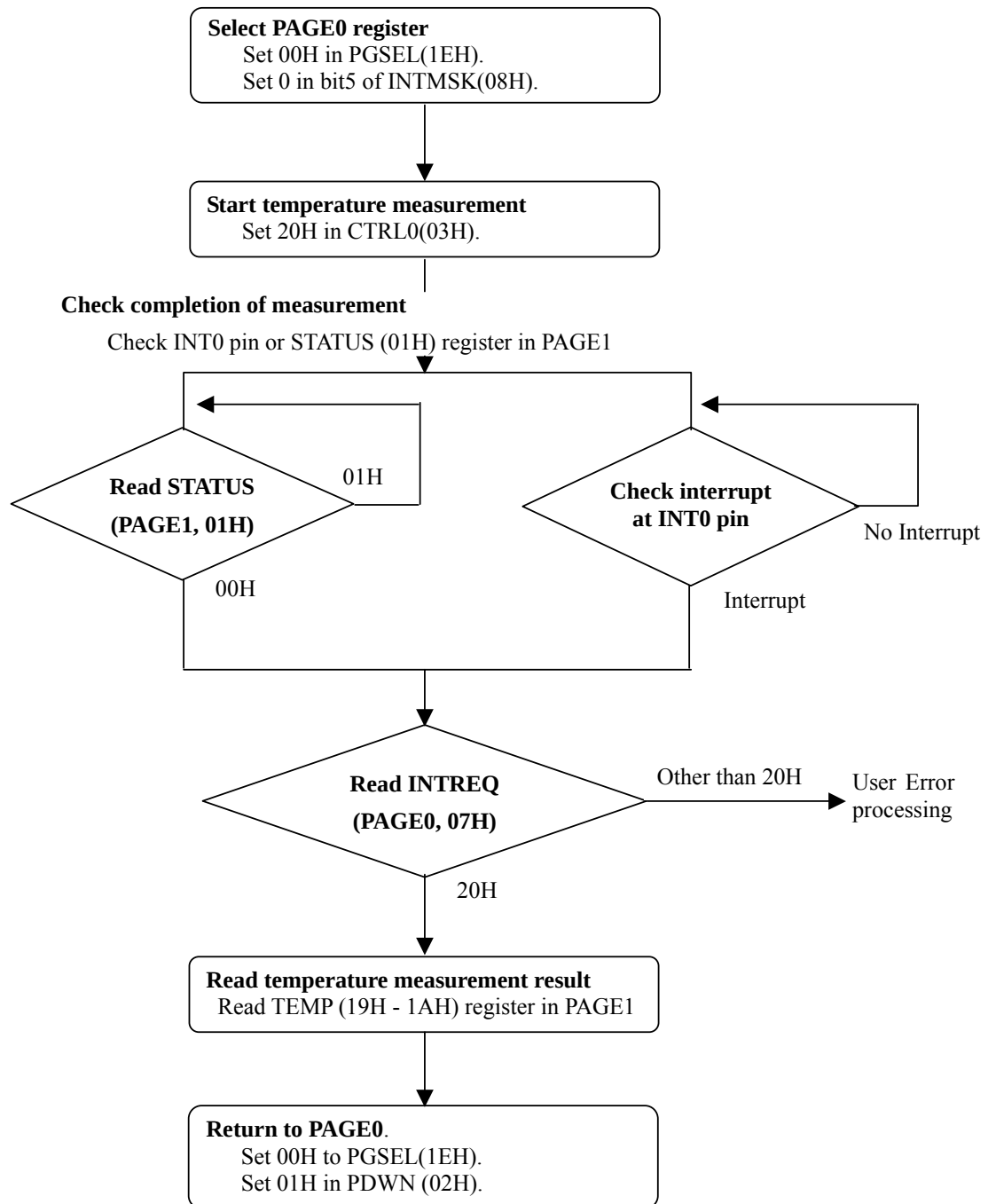
PAGE6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RSVn(0AH-11H)	RSVn[7]	RSVn[6]	RSVn[5]	RSVn[4]	RSVn[3]	RSVn[2]	RSVn[1]	RSVn[0]
Default 00H (R)								

5 GENERAL CONTROL FLOW

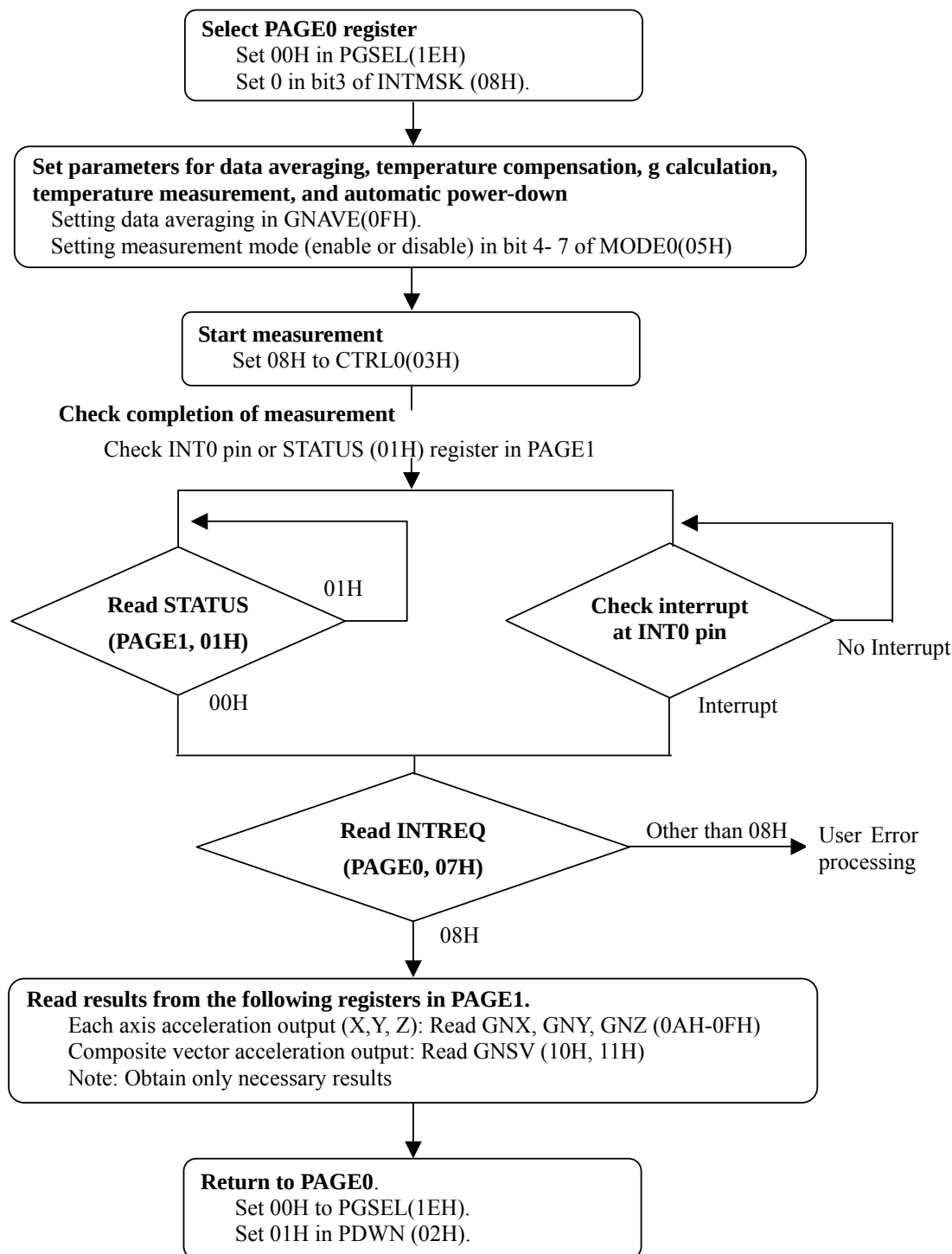
5.1 Initialization



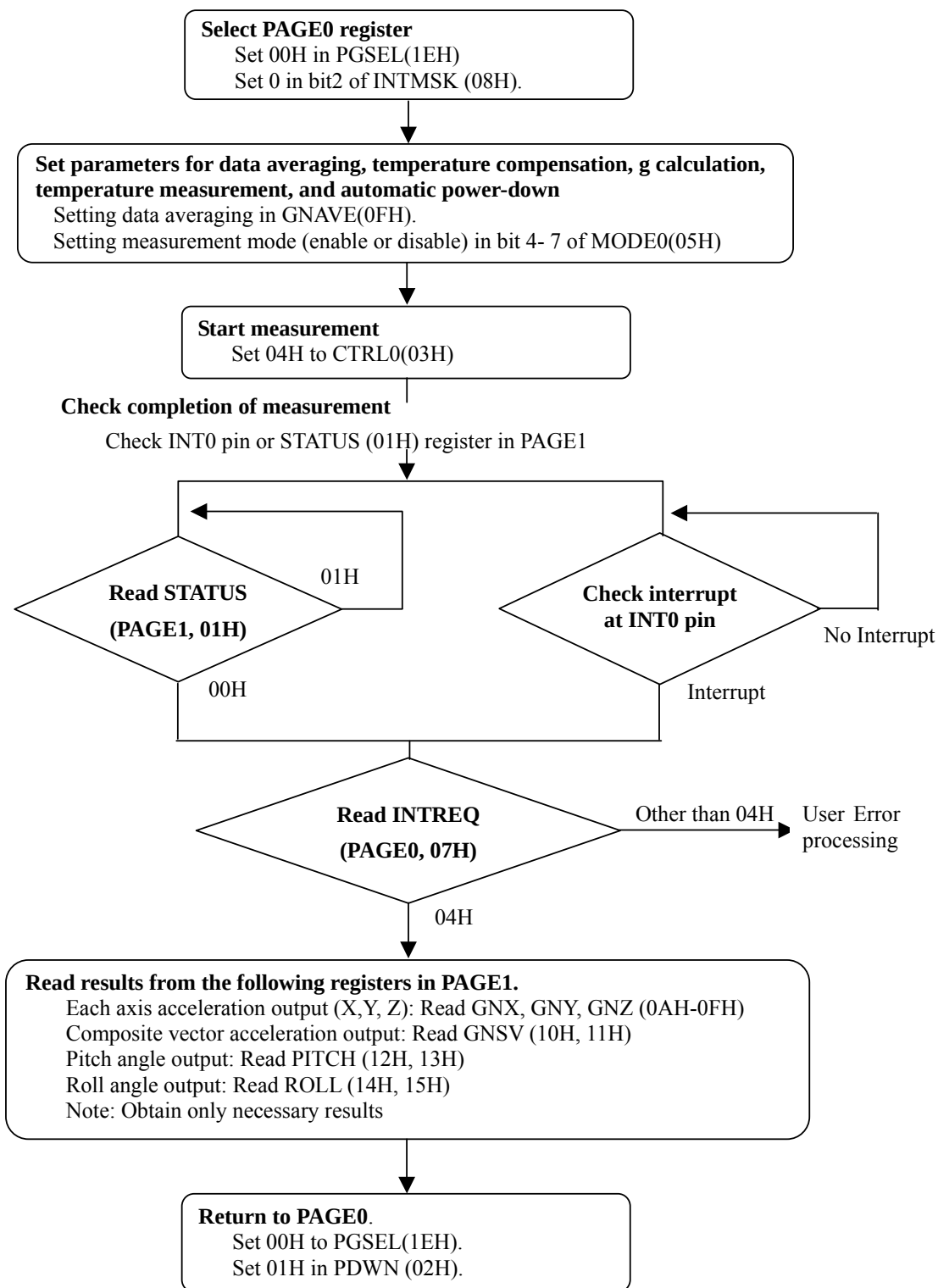
5.2 Temperature measurement



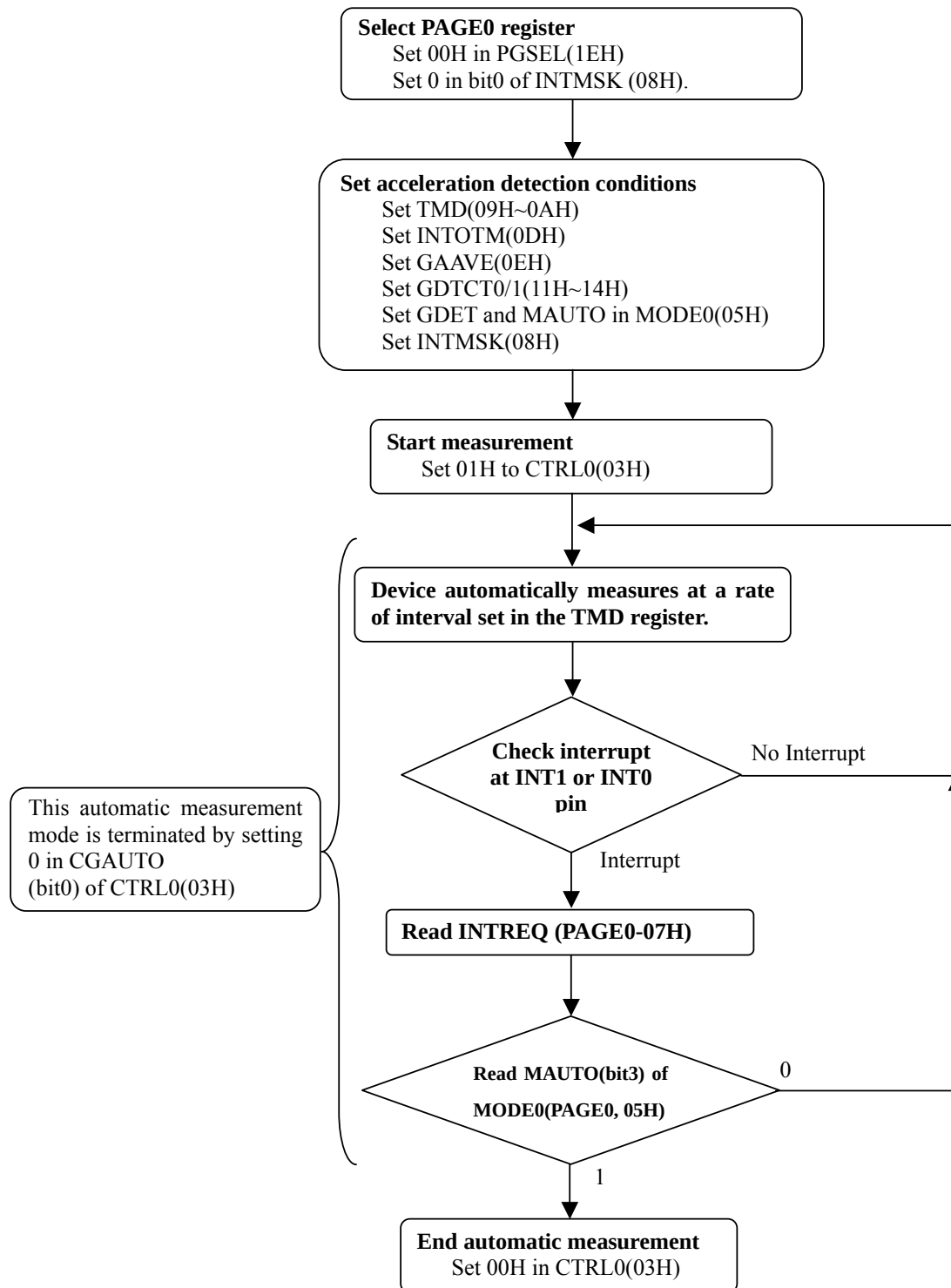
5.3 Measuring acceleration (No pitch/roll angle calculation)



5.4 Measuring acceleration (Including pitch/roll angle calculation)



5.5 Automatic measurement



Read results (PAGE1)

Set 01H in PGSEL(1EH).

Although automatic measurement is under progress, data will be obtained when setting 0 in the ASTS (bit 1) of STATUS(01H)

Read results.

Each axis acceleration output (X,Y, Z): Read GAX, GAY, GAZ (02H-07H)

Total acceleration output: Read GASV (08H, 09H)

Pitch output: Read PITCH (12H, 13H)

Roll output: Read ROLL (14H, 15H)

Note: Obtain only necessary results

Note: To calculate pitch/roll, write 1 in AGCON (bit 4) of MODE0(05H) in PAGE0.

Example of automatic measurement settings

<Setting conditions>

Free-fall detection: 0.4g

Interval: 10 ms

Detection: Three detections out of five measurements

Data averaging: 8 times

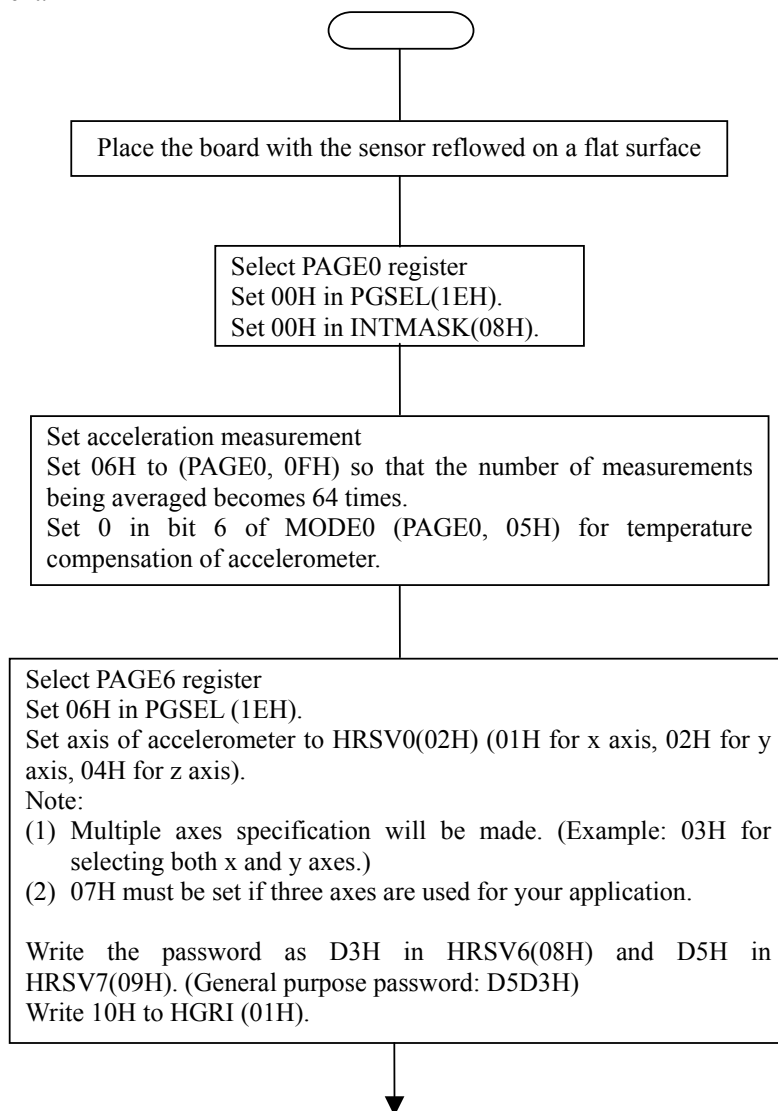
Name of register	Register address	Setting value	Description
MODE0	05H	00H (Default)	Bit7: Automatic power down is on. Bit6: Temperature compensation is enabled. Bit5: Temperature measurement is included. Bit4: No g calculation. Bit3: Continued after g detection. Bit2: - Bit1, 0: g detection range is between GDTCT1 (0g) and GDTC0 (0.4g).
TMDL	09H	1EH	10 ms
TMDH	0AH	00H	10 ms
GDTCT0L	11H	9AH	0.4g
GDTCT0H	12H	01H	0.4g
GDTCT1L	13H	00H	0g
GDTCT1H	14H	00H	0g
INTOTM	0DH	35H	NMR = 3, DNM = 5
GAAVE	0EH	03H	Data averaging: 8 sampling times

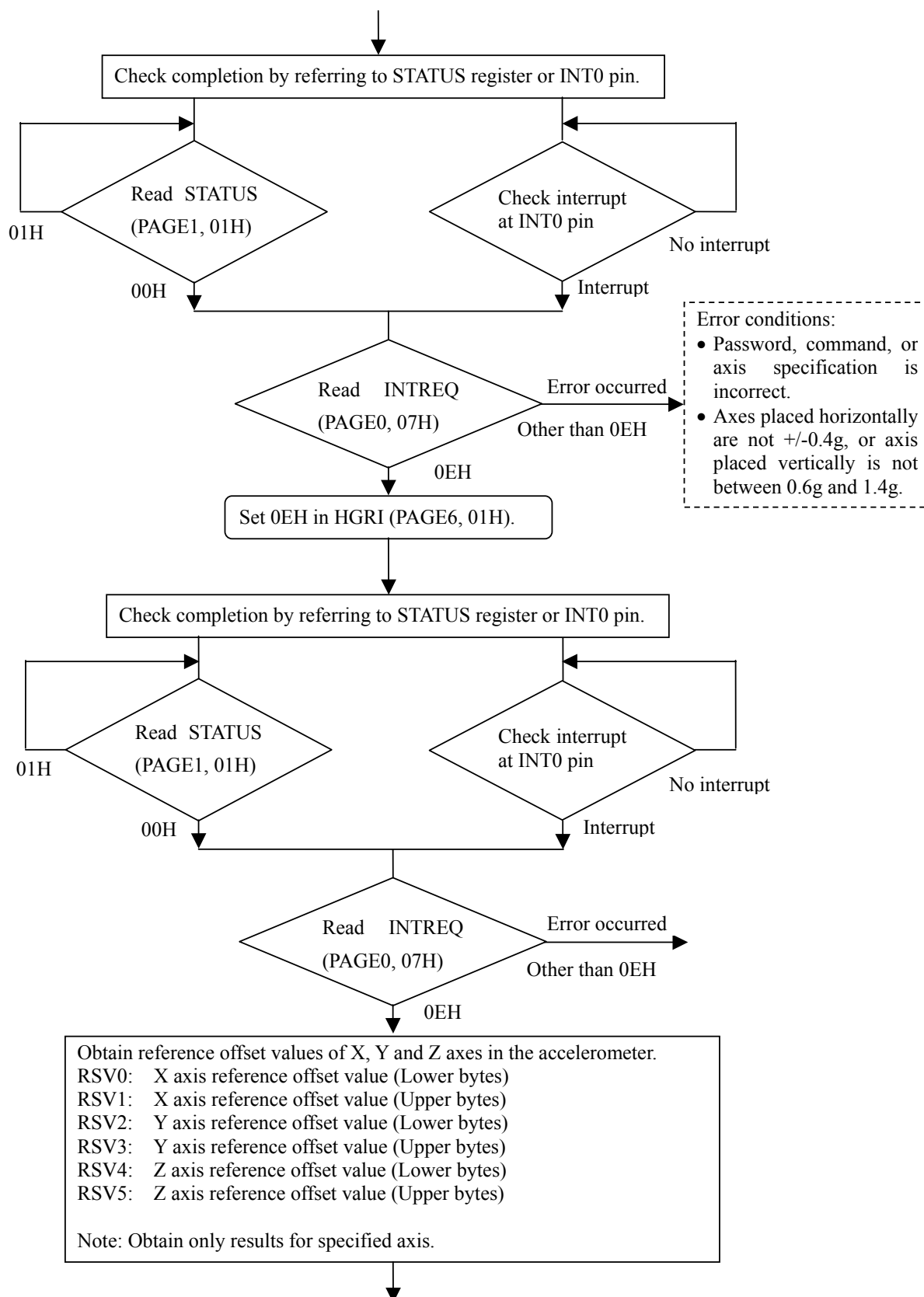
5.6 Offset adjustment

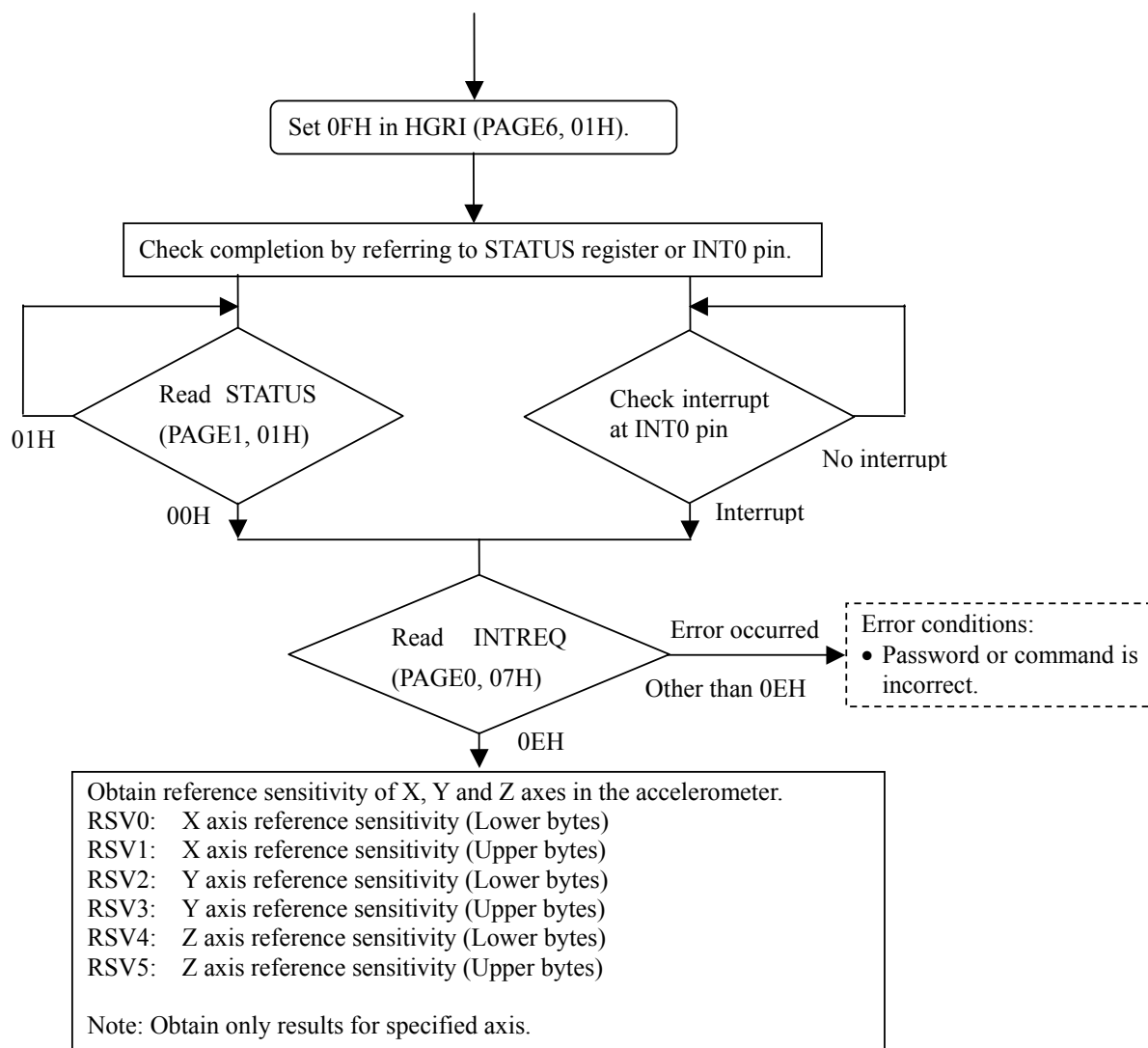
The ML8953A is factory-calibrated, however, on rare occasion an offset shift may occur upon soldering on PCB due to the device being skewed in relation to the PCB plane. Most applications might allow such small offset, but for applications that can not tolerate such offset, this section provides a guide to bring the offset shift back to near factory calibrated offset values. The offset adjustment will be simply performed at customer's site. This procedure is also applicable to readjust in-use offset shift if in case the offset shift is beyond tolerance of your application. The methods in 5.6.1 and 5.6.2 must be performed.

5.6.1 Performing offset adjustment

The following flow chart shows the procedures of offset adjustment. Please remember to perform the adjustment more than 12 hours later after reflowing components on PCB. The PCB must be placed on a flat surface during the adjustment.





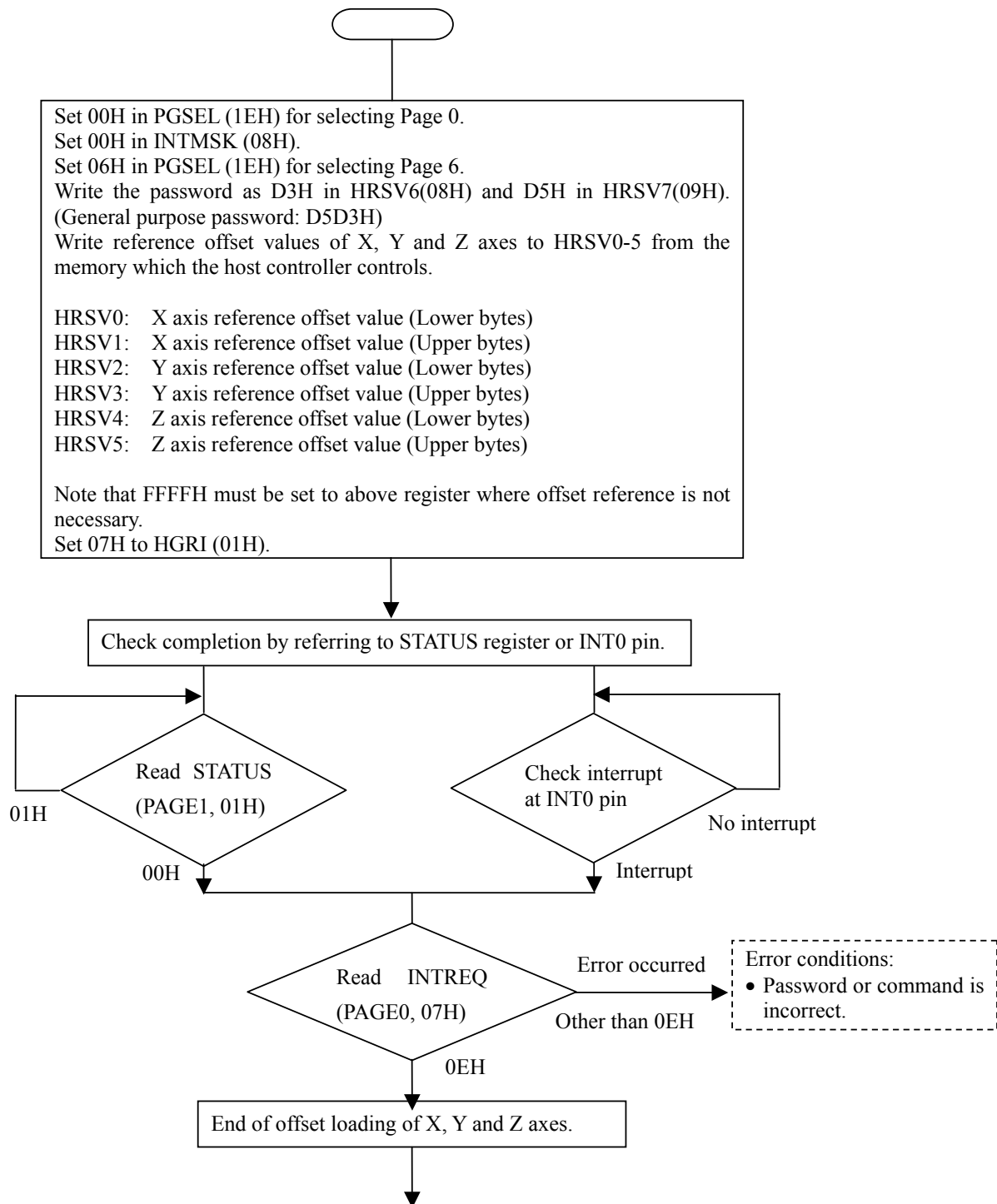


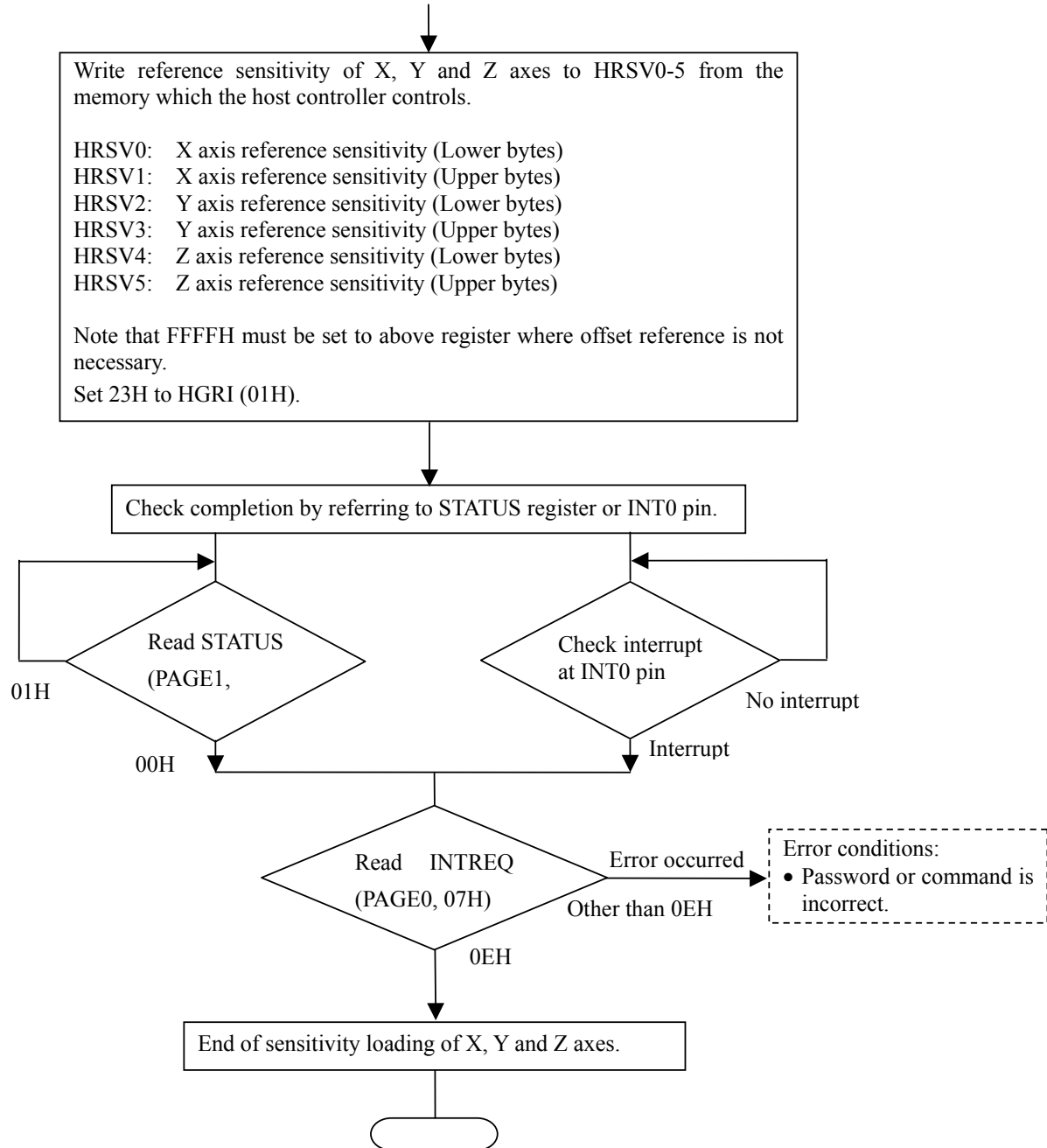
Note:

- Reference offset and sensitivity are valid until power is turned off.
- Reference offset and sensitivity must be stored in memory which a host controller controls.
- If power is turned off, the reference offset and sensitivity will be erased. Thus, it is necessary to reload the offset and sensitivity stored in the memory by using PAGE6 commands every time power is turned on. The reloading method is provided in the next section.

5.6.2 Loading of reference offset and sensitivity in re-powering up

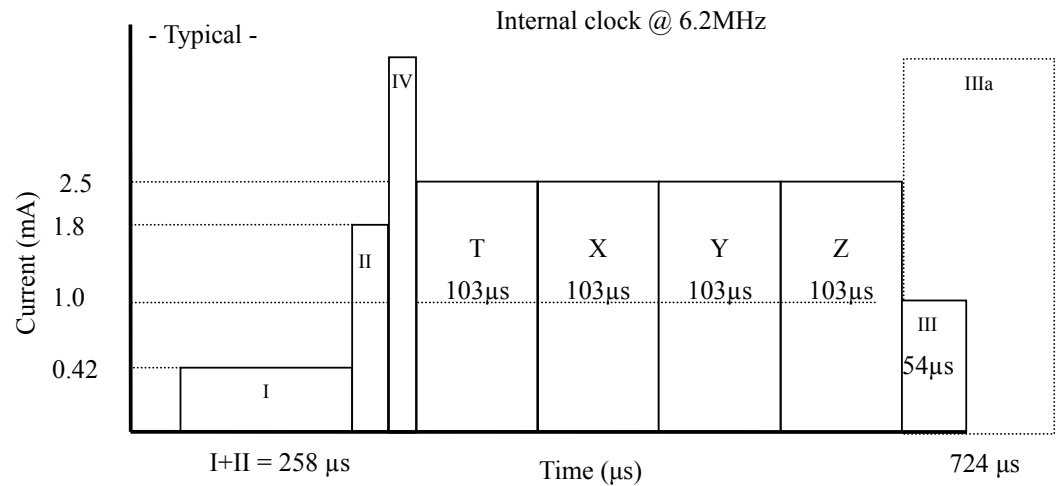
Offset and sensitivity reference values must have been stored in by the host controller in memory.





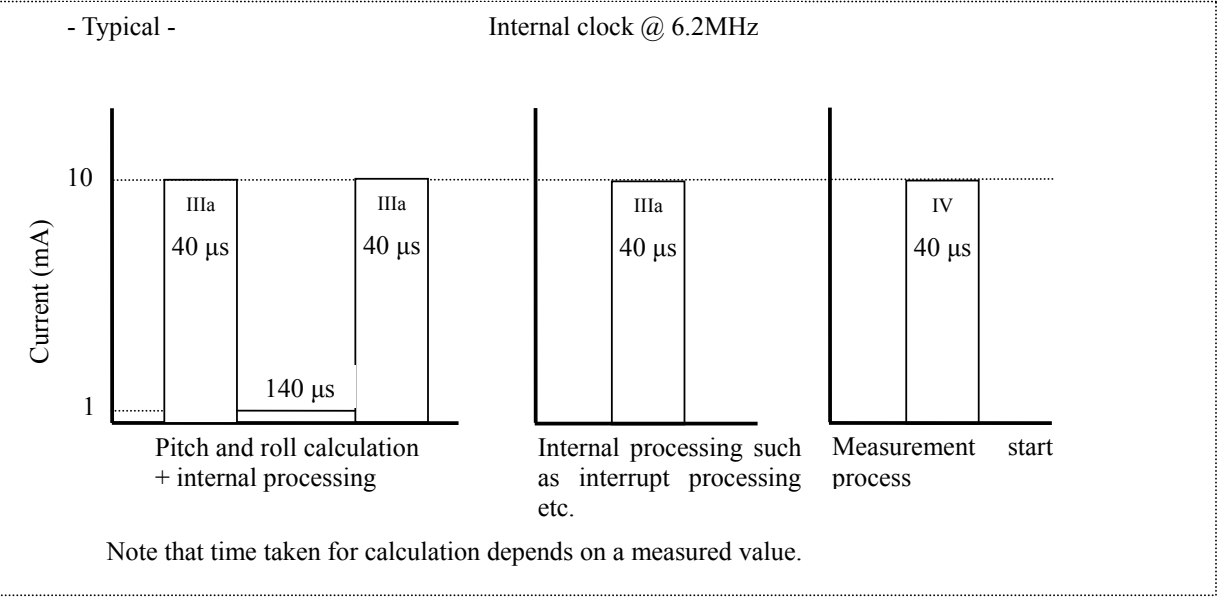
6 ELECTRIC CHARACTERISTICS

6.1 Current consumption diagram in acceleration measurement (Including calculation)

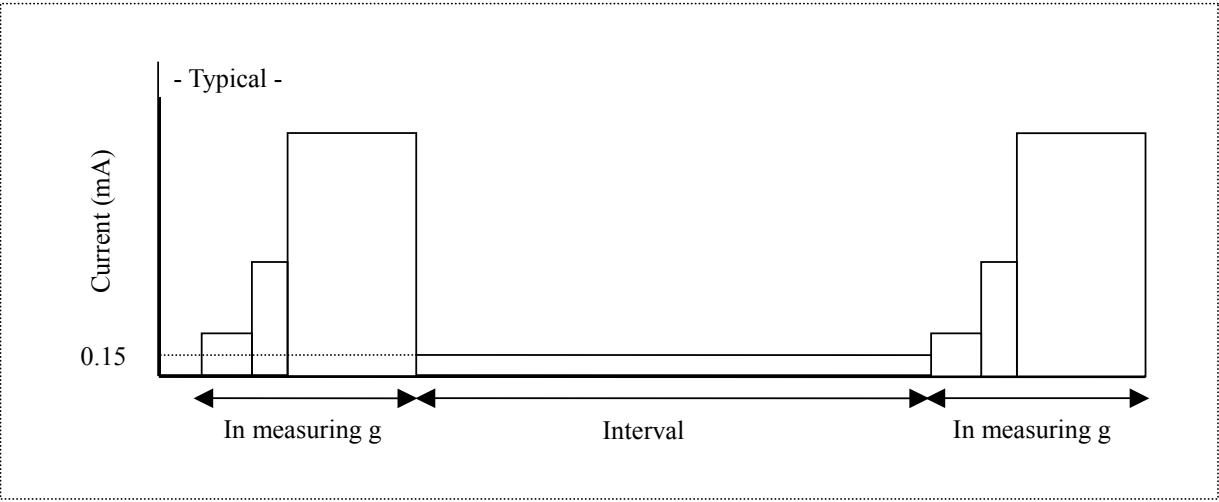


- (I) VREF/BIAS = ON
- (II) DA/AD/OSC/GS = ON
- (III) g calculation = ON, No pitch and roll calculation
- (IIIa) g calculation = ON, Including pitch and roll calculation. Refer to the corresponding diagrams in section 6.2.
- (IV) Measurement start process. Refer to the corresponding diagrams in section 6.2.

6.2 Diagram of current consumption in calculation

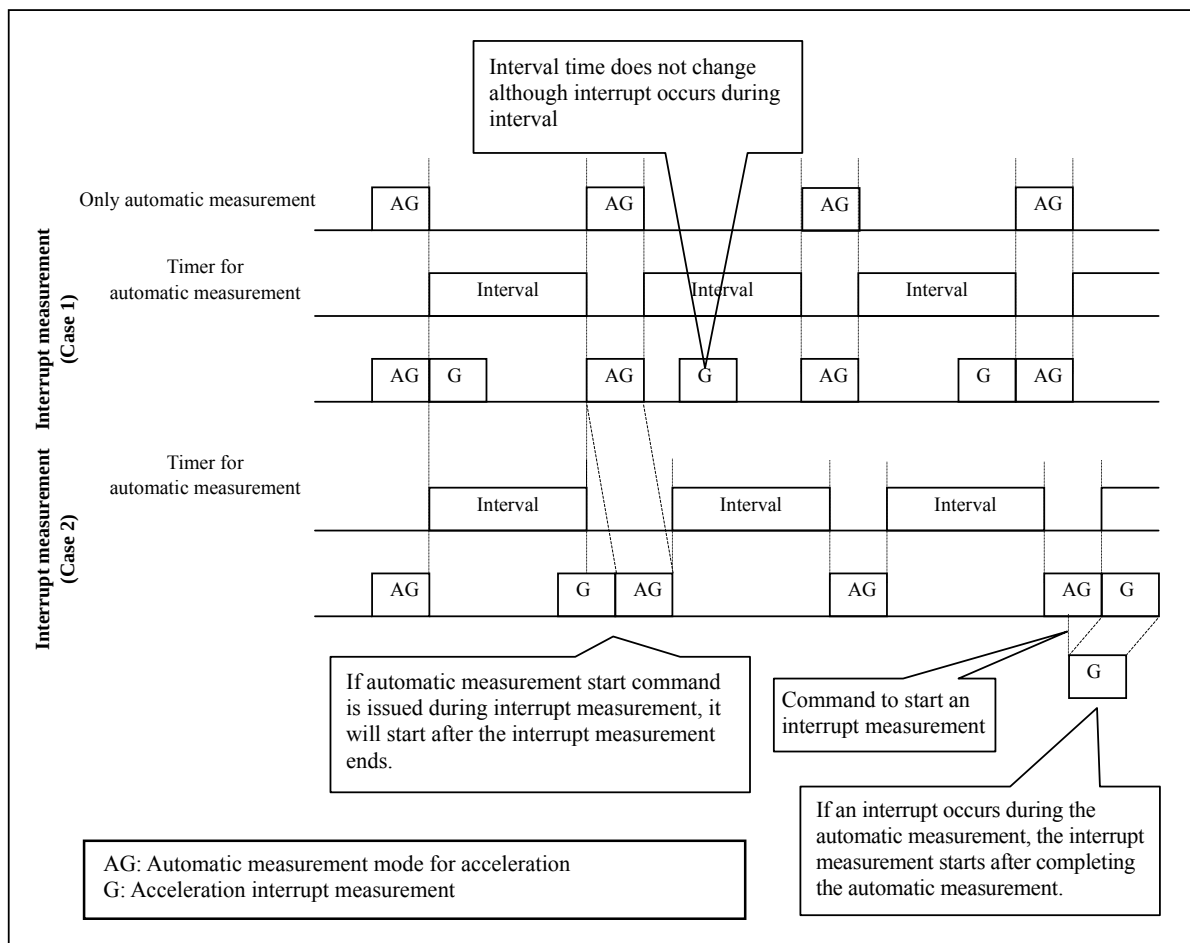


6.3 Diagram of current consumption in automatic measurement during interval between measurements



7 AUTOMATIC ACCELERATION MEASUREMENT MODE AND INTERRUPT MEASUREMENT

In the automatic acceleration measurement mode, it is possible to interrupt measurements of accelerometer.



Automatic measurement and interrupt measurement

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDK8953A-04AFC	Mar 10, 2008	–	–	Preliminary edition 1

Document Disclaimer

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.
4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.
5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.
6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by Oki, authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.
7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.
8. This sensor contains a mechanical sensitive part. Improper handling may cause permanent damages to the device. Although the device is permanently damaged, please ensure to provide the system level safety measures to prevent direct or indirect personal injury, death, or damages to assets.
9. No part of the contents contained herein may be reprinted or reproduced without our prior permission.