BUGBASE VIDEO PIM

VERSION HISTORY

VER #	DATE	ACTION	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	25 SEPT 2009	DRAFT	DRAFT	HARSHITH	-----	-----
0.02	21 OCT 2009	UPDATED IIR_001 COMMENTS	1. VGA CONNECTOR CHANGED TO A THIN CONNECTOR. 2. VBAT TO 5V CHARGE PUMP ADDED. 3. 0E_1% RESISTORS CHANGED TO 0E_5%. 4. SEVEN 0E_1% RESISTORS CHANGED TO 0E_5%. 5. 0E REMOVED FROM EEPROM SUPPLY. 6. CHANGED HDMI SUPPLY TO 5V. 7. 10uF CAP ADDED FOR TFP410 VREF RES DIVIDER SUPPLY. 8. 3.3V TO 5V I2C LEVEL TRANSLATOR ADDED FOR DDC I2C. 9. FUSE CHANGED TO 62.5mA PART. 10. RESISTOR DIVIDER ADDED FOR HOT PLUG CIRCUIT. 11. S-VIDEO TEST POINTS REMOVED. 12. CH7026 CHIP REPLACED BY THS8200 AND THE RELATED FILTER CIRCUITS CHANGED. 13. 2.5V LDO REMOVED. 14. SUPPLY FILTER BEADS CHANGED TO 0603 PART. 15. DNI STRAP OPTIONS PROVIDED ON TFP410 I2C LINES. 16. 0E RESISTORS INCLUDED ON TFP410 I2C LINES.	HARSHITH	AVINASH, PRASAD ACHAR	AVINASH
1.00	23 OCT 2009	UPDATED IIR_002 COMMENTS AND BASELINED	1. PU-PD option provided on TFP410 ISEL pin. 2. Text table explaining the GPIO operation added. 3. Text table for default TFP410 settings added. 4. Hot plug resistor divider circuit removed and incorporated a level shifter design. 5. 0E option provided on VGA DDC lines. 6. The PD resistor on VGA_nRESETB line in the schematic is shifted to near the encoder. 7. Block diagram updated with THS8200. 8. 75E parallel termination added at the source on VGA RGB lines. 9. Supply connected to VDD_DLL of THS8200 through a filter. 10. Added 0.01uF de-caps for all the IC power supplies. 11. VGA & HDMI connector body connected to GND through a bead. 12. Added VGA port protector cum HSYNC, VSYNC, I2C level translator and removed existing level translation and protection circuit. 13. Added ESD filter on HDMI DDC I2C lines. 14. Connected Pull-up resistors of TFP410 to VDD_3V3 from AVDD_3V3. 15. Changed TFP410 Vref circuit to use 1K resistors.	HARSHITH	AVINASH, PRASAD ACHAR, SOUMYA	AVINASH
1.01	30 OCT 2009	UPDATED	1. Series termination added on DSS signals. 2. Fuses for VGA and HDMI connector changed to PPTC part. 3. Added table with resistor DNI for default operation. 4. Added two more HDMI filters and modified circuit to use one HDMI filter per signal pair. 5. Added two I2C buffers and a Not gate for selection between EEPROM and VGA DDC.	HARSHITH	-----	-----
2.00	06 NOV 2009	UPDATED IIR_003 COMMENTS AND BASELINED	1. Series termination added on DSS_VSYNC and DSS_ACBIAS signals. 2. Modified PIM connector connections to include HDMI MSEN. 3. Both VGA and DVI chipset controlled by a single reset through a NOT gate. 4. Bead added between VGA connector body and GND.	HARSHITH	PRASAD ACHAR	AVINASH
2.01	15 FEB 2010	MODIFIED TO CORRECT BUGS OF REV-A	1. Added 10K Pull-down resistor for HTPLG AND gate input. 2. I2C address isolation taken care of by using a I2C 4-port switch. 3. Nomenclature of signals changed to use DVI instead of HDMI	HARSHITH	-----	-----
2.02	23 FEB 2010	UPDATED IIR COMMENTS	1. Switch eliminated for TFP410 I2C. 2. PCA9546 replaced with PCA9543 2-port switch and I2C level translator added for THS8200.	HARSHITH	AJIT	AVINASH
2.03	01 MAR 2010	CHANGED	1. Added I2C I/O expander. 2. Not gate ICs removed. 3. Dual LED added. 4. DVI reset, I2C switch reset, LED controls and EEPROM select control realized through I/O expander. 5. Removed pull - up & pull - down options on TFP410 address lines and added a single pull - down DNI option. 6. Changed I2C I/O expander I2C address. 7. VGA outputs at 0.7V made default at power-up.	HARSHITH	-----	-----

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BUGBASE VIDEO PIM

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REV	B
VERSION	2.03

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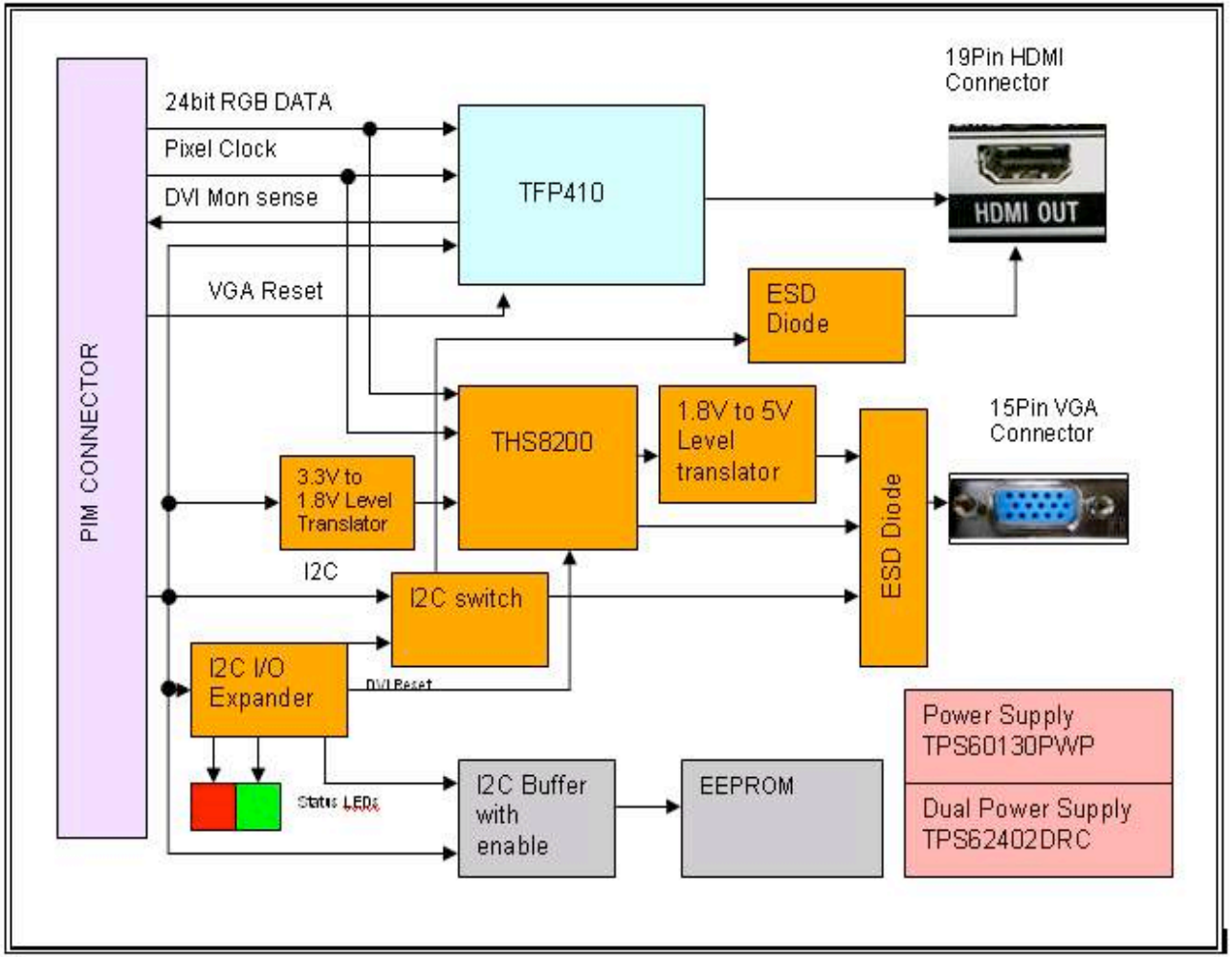
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BLOCK DIAGRAM



I2C SLAVE ADDRESS

DVI CHIPSET (TFP410)	**0x70, 0x71**
EEPROM (AT24C02)	**0xA0, 0xA1**
VGA ENCODER (THS8200)	**0x40, 0x41**
DVI DDC	**0xA0, 0xA1**
VGA DDC2B	**0xA0, 0xA1**
VGA DDC2AB/DDC2B+	**0x6E**
I2C SWITCH (PCA9543AP)	**0xE2, 0xE3**
I2C I/O EXPANDER (PCA9554P)	**0x42, 0x43**

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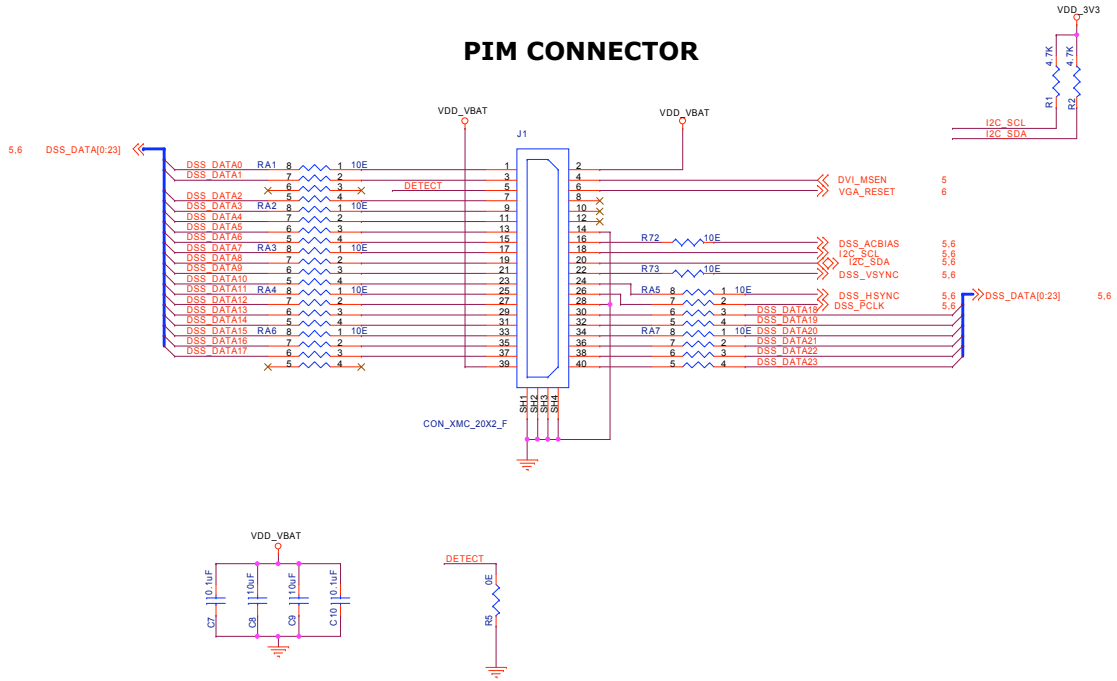
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Title **BLOCK DIAGRAM**

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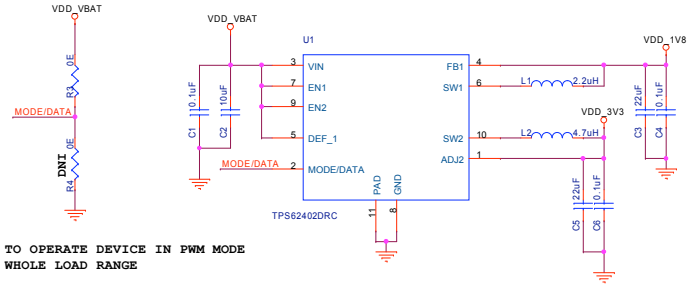
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PIM CONNECTOR



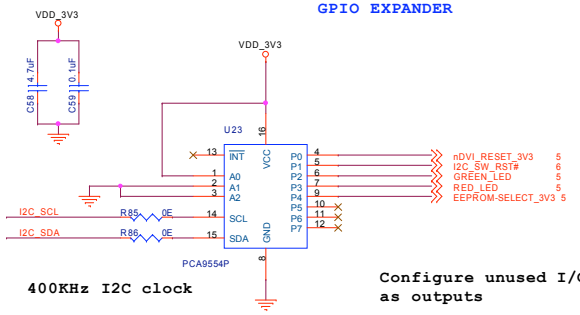
BUCK CONVERTER

VDD _1V8 -> 1.8V/400mA
VDD _3V3 -> 3.3V/600mA



MOUNT R3 TO OPERATE DEVICE IN PWM MODE OVER THE WHOLE LOAD RANGE

GPIO EXPANDER

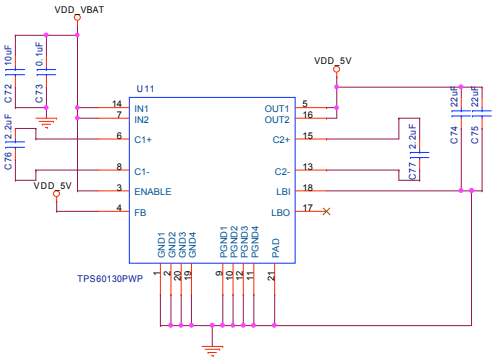


400KHz I2C clock

Configure unused I/Os as outputs

CHARGE PUMP

VDD _5V -> 5V/300mA



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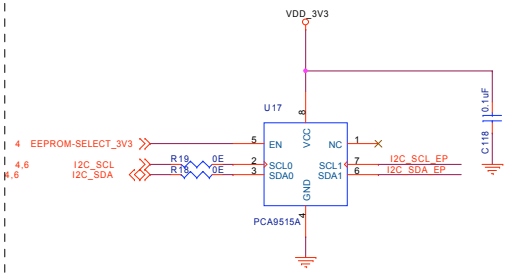
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Title **POWER, PIM CONNECTOR**

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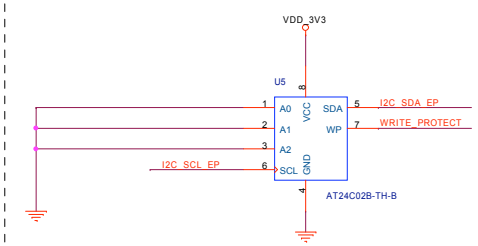
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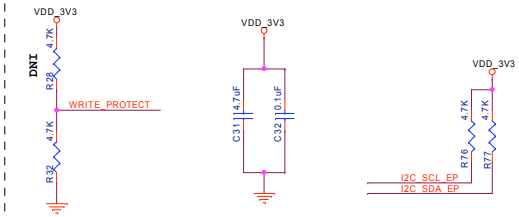
DVI Interface

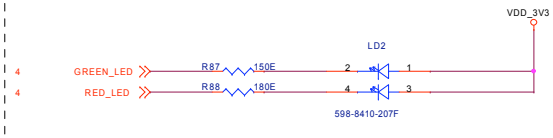


I2C BUFFER TO ISOLATE EEPROM WHILE ACCESSING MONITOR EEPROMs

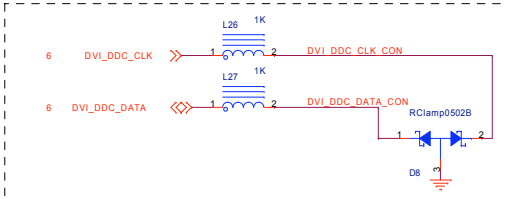
EEPROM - 2K

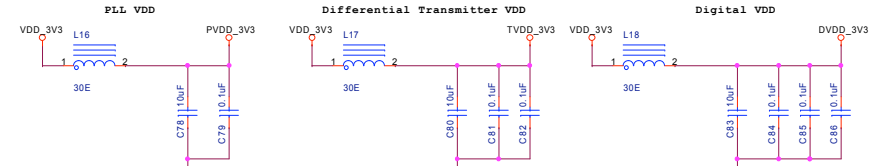


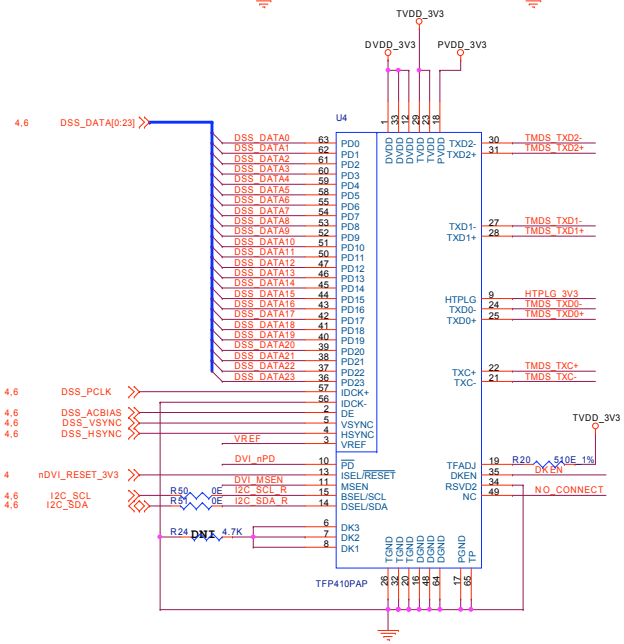




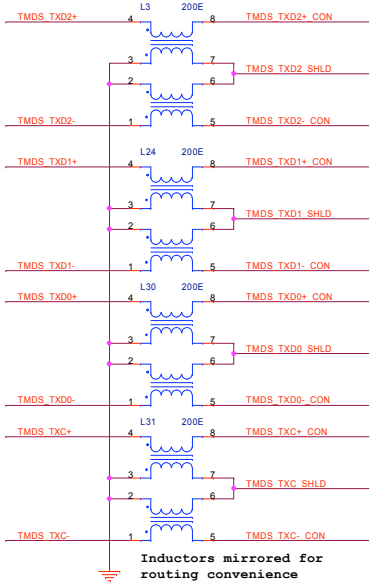
STATUS LED





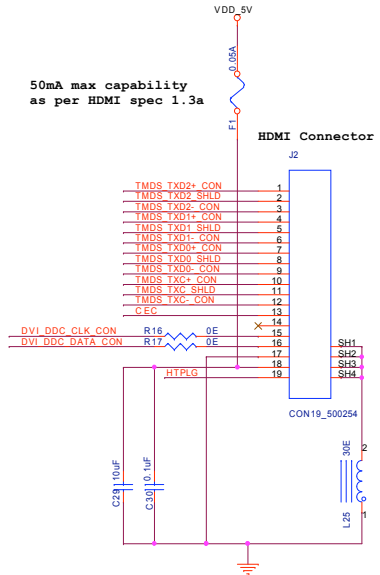


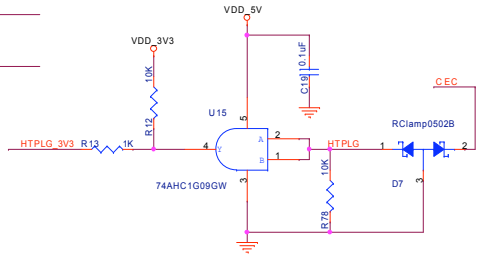
All TMDS lines are to be routed as differential pairs with 50E impedance.



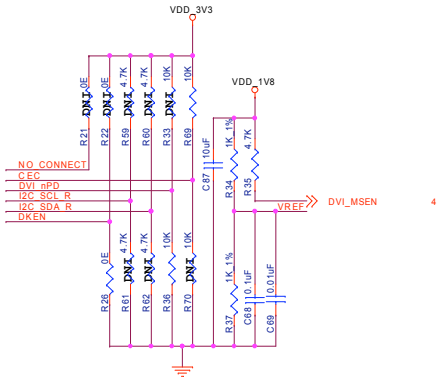
Inductors mirrored for routing convenience

50mA max capability as per HDMI spec 1.3a





Level translation for Hot Plug Detect



Resistor connections

1	R29, R30, R31 MOUNTED TO MAKE TFP410's I2C ADDRESS 0x70 & 0x71
2	R36 MOUNTED WHEN USING TFP410 IN I2C CONFIG MODE
3	R59, R60, R61, R62 TO BE USED WHEN TFP410 IS NOT REQUIRED TO BE OPERATED IN I2C MODE. R51 AND R51 HAS TO BE MADE DNI IN THIS CONDITION
4	R69 AND R70 ON CEC (CONSUMER ELECTRONIC CONTROL) USED TO PROVIDE A DEFAULT LEVEL TO OTHER CEC ENABLED DEVICES
5	EITHER R26 OR R22 TO BE MOUNTED ON DKEN TO AVOID FLOATING INPUT ON DATA DE-SKEW ENABLE PIN. DE-SKEW CONTROLLED THROUGH I2C

VIDEO FORMAT ON TMDS

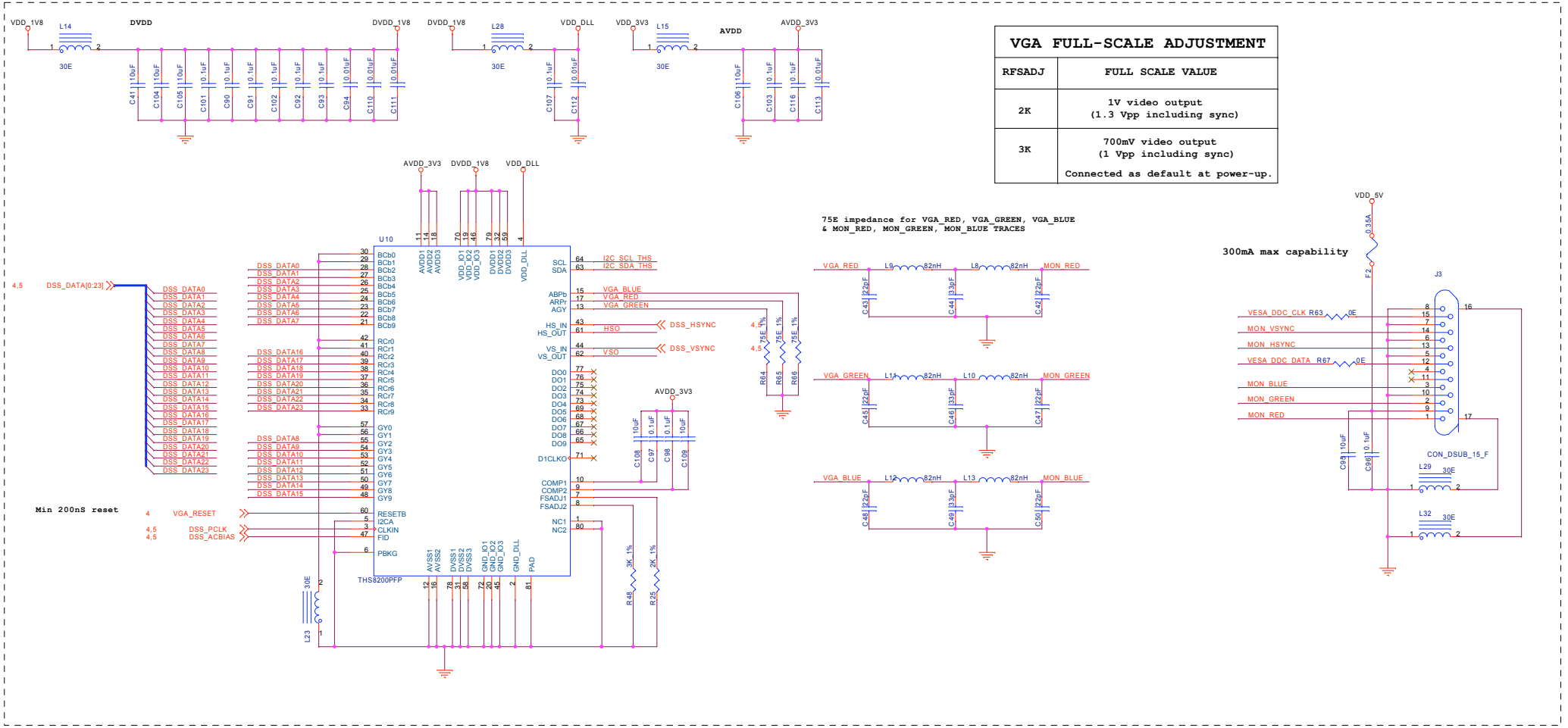
CHANNEL	DURING ACTIVE VIDEO	DURING BLANKING INTERVAL
TXD0±	BLUE	HSYNC & VSYNC
TXD1±	GREEN	CTL[1] (If used)
TXD2±	RED	CTL[3:2] (If used)
TXC±	CLOCK	CLOCK

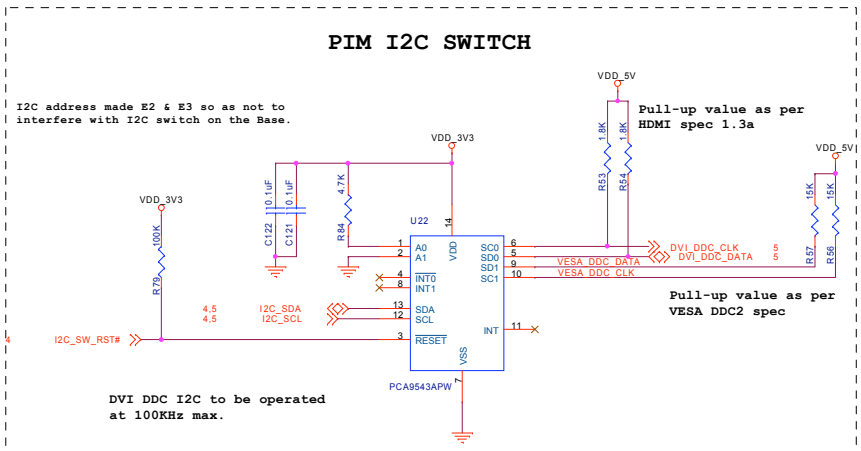
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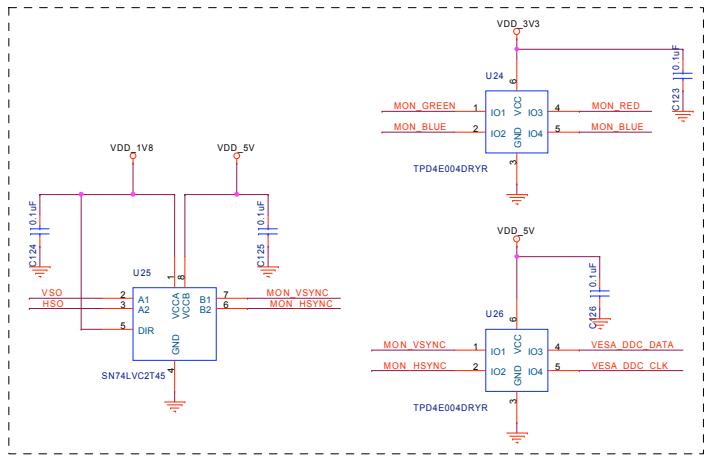
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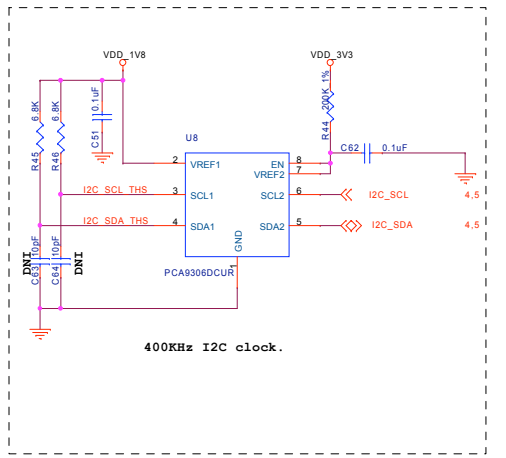
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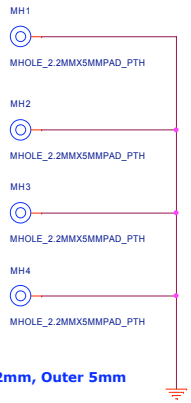
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Title: VGA

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MOUNTING HOLES



Mounting holes PTH Inner 2.2mm, Outer 5mm

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ACCESSORIES

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