

BugLabs General PCB Fab Notes:

1) Substrate Material:

- a) Polyclad 370 HR (RoHS compliant material). Glass transition temperatures must meet or exceed the temperatures associated with lead free assembly processes.

2) PCB Specification/Requirements:

- a) This fabrication should be "RoHS Compliant".
- b) Fabricate to IPC-A-600, current revision.
- c) Inspect per IPC-A-600, Class 2, current revision.
- d) Board shall have a UL rating of 94V-0.

3) Mechanical Tolerances and Specifications:

- a) All dimensions are in mm (unless otherwise specified).
- b) Layer-to-layer registration shall be .008" True Position within a given PCB stackup (all layers).
- c) Overall board thickness to be $\pm 10\%$ nominal requirement (measured over final finish).
- d) Finished PCB warpage and twist per IPC-6012.
- e) Weight of all copper layers shall be not less than 1 oz.
- f) All hole diameters are finished sizes.
- g) Copper Plate .001" minimum average in the PTH's.
- h) Plated through component hole tolerances to be ± 0.003 " (unless otherwise specified).
- i) Plated through via hole tolerances to be ± 0.003 " Nominal (unless otherwise specified).
- j) Non-Plated holes to be ± 0.002 ".
- k) Minimum allowed conductor width is 6 mil. Minimum allowed conductor spacing is 6 mil.
- l) Vias shall be directly connected to the respective plane.
- m) Add thermal relief with appropriate science on all direct hit drills.
- n) Tolerances for dimensions shall be: .XX ± 0.020 " .XXX ± 0.010 " (unless otherwise specified).
- o) Internal cutouts, maximum inside radii shall be .062" R (.0465" R typical).
- p) If required, chamfered board corners should be 45°.
- q) Beveled tips should be 45° and about .030" deep ($\pm .005$ ").
- r) If required, V-Score using a 30° angle, to leave .015" $\pm .003$ " or 30% remaining (whichever is greater).
- s) Remove all burrs and break sharp edges .015" max.

4) Electrical Test:

- a) 100% of boards shall be electrically tested for continuity.

5) Controlled Impedance:

- a) Impedance to be $\pm 10\%$ (if required by conformance). Geometric structures specified on the cross section/stack-up are for reference only. Impedance is the controlling parameter for the stackup.

6) Finish:

- a) Gold immersion (unless otherwise specified).

7) Soldermask:

- a) Soldermask both sides with Liquid Photo Imageable (Green) per IPC-SM-840.
- b) Soldermask over bare copper (SMOBC).
- c) LPI soldermask Taiyo PSR4000 HFX (RoHS compliant material) or equivalent.
- d) Soldermask registration to be within diametrical true position of ± 0.002 " with applicable hole/pad.

8) Silkscreen:

- a) Silkscreen shall be White-Haven PC421 (non-conductive) or equivalent RoHS compliant material), both sides (unless otherwise specified).
- b) Clipping of characters allowed to achieve no Silkscreen on exposed solderable land areas or pads.

9) Marking:

- a) Manufacturer's UL logo and lot traceability shall be marked far side (in etch or legend) (unless otherwise specified). Maximum height is 0.120".
- b) 94V-0 rating shall be marked far side.

10) Teardropping:

- a) Teardropping or snow-manning or filleting shall be permitted on inner layers to insure a 2-mil wide electrical path at the pad to trace junction.